

PROJECT NAME : CAL51/CLA61/CAL71
PCB NO :

Dell / Compal Confidential

Schematic Document

AMD Raven

AMD R17M-M2-50 (23 X 23mm) +GDDR5 x4

2017-10-30 Rev: 1.00 (A00)

@ : Un-pop Component

R5_PC@/R7_PC@/R3_PC/R5_PR@/R7_PR@/R5_PR_R3@/R7_PR_R3@:APU PN

45@: HDMI LOGO

PCB@/: MB part number

4G_S@/4G_M@/4G_H@/2G_H@/2G_M@/2G_S:

VRAM Strap Pin:

Vram 2G:S2G_R3@ / H2G_R3@ /M2G_R3@

Vram 4G:S4G_R3@ / H4G_R3@ /M4G_R3@

DIS@: GPU only

M50_R3@:GPU R3 PN

UMA@/:UMA only

TI@/PARADE@/NRDSA@ : SATA

3234@ :Audio

EMI@/ESD@/RF@ : EMI, ESD ,RF Component

@EMI@/@ESD@/@RF@ : EMI, ESD,RF unpop

KBBL@:for KB backlight use

PTP@/NPTP@/TP_WAKE@:Touch pad

TYPEC@/NOTYPEC@:TYPEC

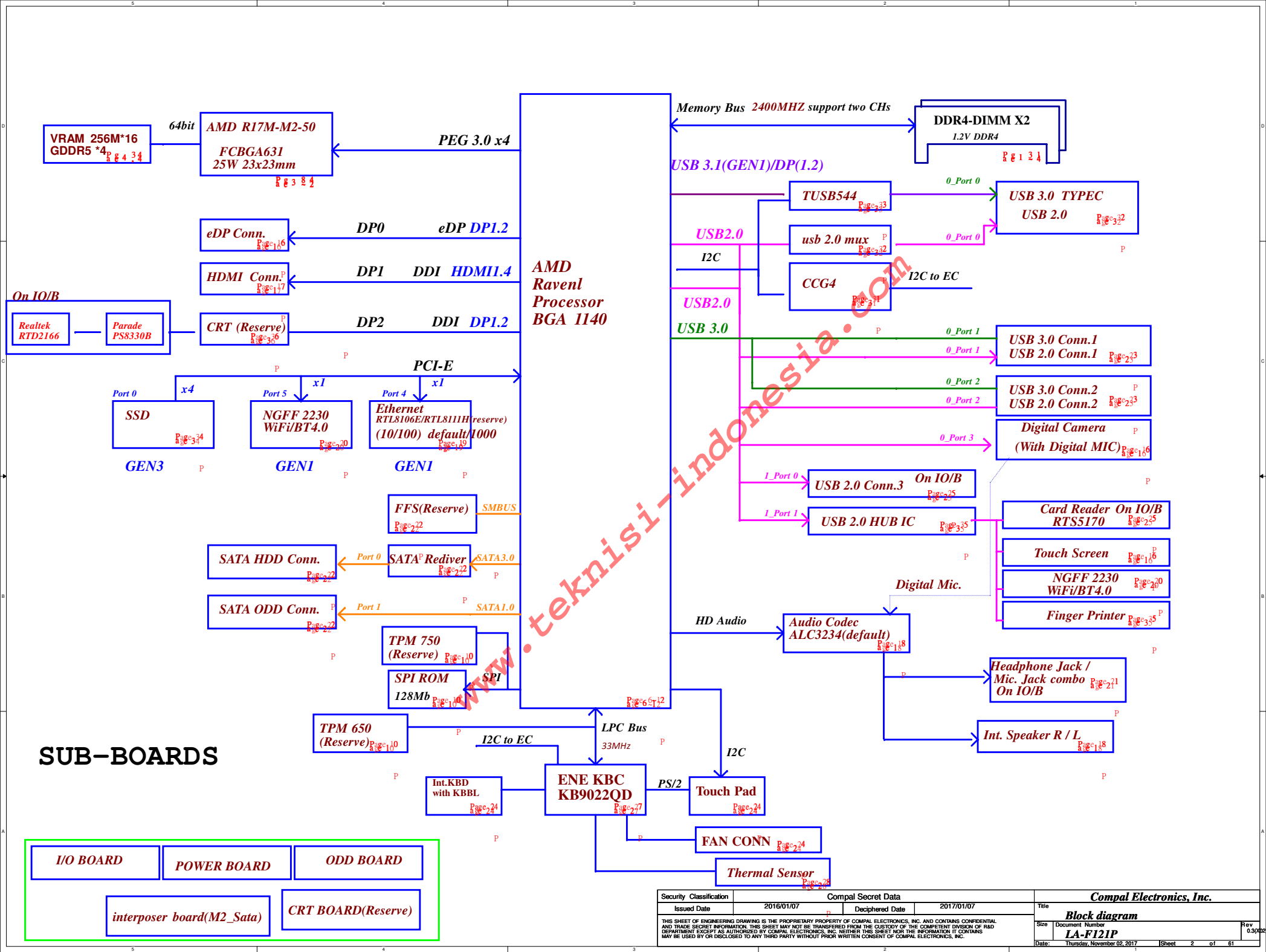
Typec@EMI@/Tyepc@ESD@: EMI/ESD typec component

CRT@:D-sub TPM@:TPM FFS@:free fall sensor

HDT@ /Debug use

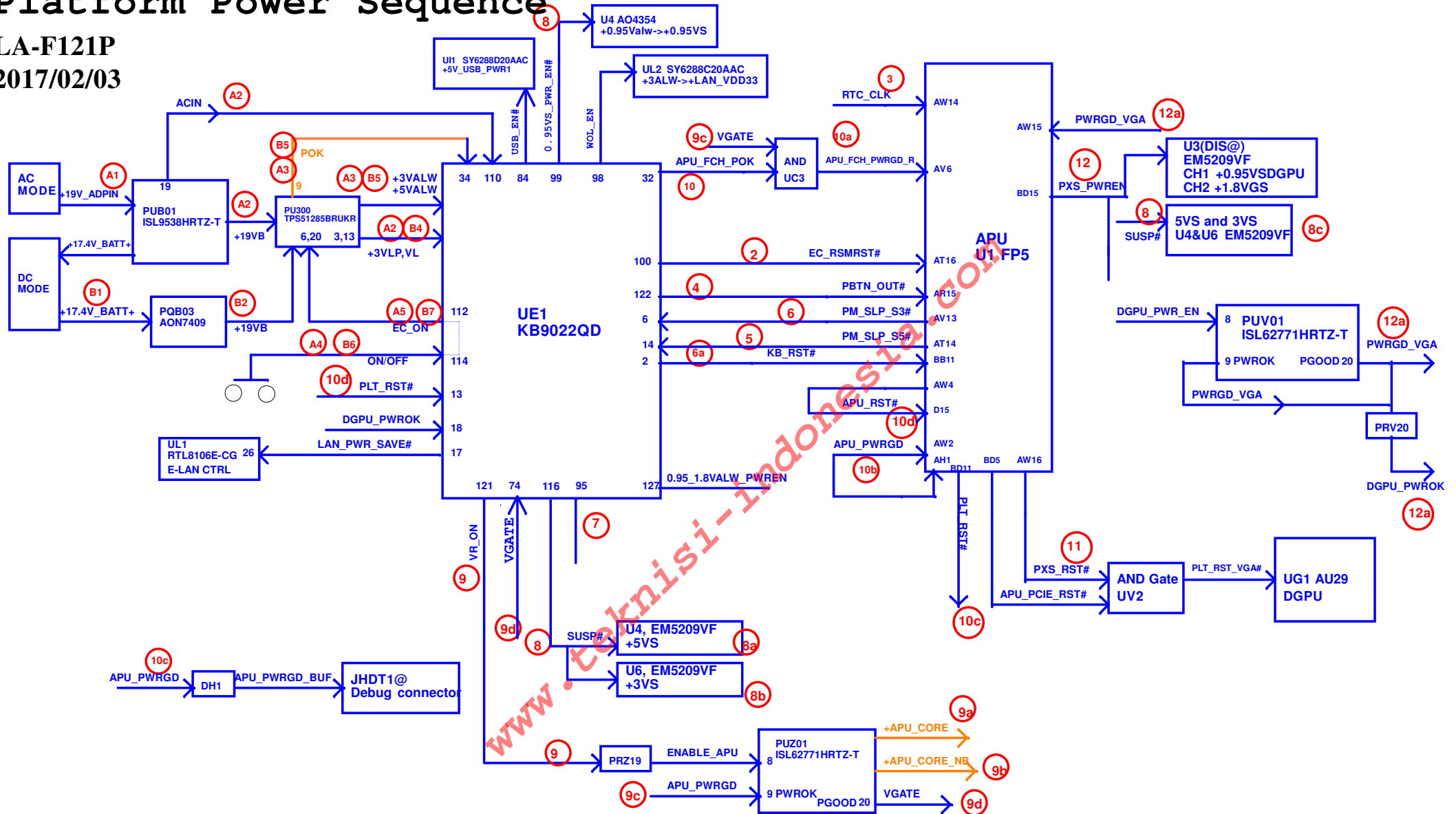
MODS@:moderd standby

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Platform Power Sequence

LA-F121P
2017/02/03



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Board ID Table for AD channel

Vcc	3.3V +/- 1%				
Ra	100K +/- 1%				
Board ID	Rb	Vao aio min	Vao aio typ	Vao aio max	EC AD3
0	0	0.000V	0.000V	0.300V	0x00 - 0x13
1	12K +/- 1%	0.347V	0.354V	0.360V	0x14 - 0x1E
2	15K +/- 1%	0.423V	0.430V	0.438V	0x1F - 0x25
3	20K +/- 1%	0.541V	0.550V	0.559V	0x26 - 0x30
4	27K +/- 1%	0.691V	0.702V	0.713V	0x31 - 0x3A
5	33K +/- 1%	0.807V	0.819V	0.831V	0x3B - 0x45
6	43K +/- 1%	0.978V	0.992V	1.006V	0x46 - 0x54
7	56K +/- 1%	1.169V	1.185V	1.200V	0x55 - 0x64
8	75K +/- 1%	1.398V	1.414V	1.430V	0x65 - 0x76
9	100K +/- 1%	1.634V	1.650V	1.667V	0x77 - 0x87
10	130K +/- 1%	1.849V	1.865V	1.881V	0x88 - 0x96
11	160K +/- 1%	2.015V	2.031V	2.046V	0x97 - 0xA4
12	200K +/- 1%	2.185V	2.200V	2.215V	0xA5 - 0xAF
13	240K +/- 1%	2.316V	2.329V	2.343V	0xB0 - 0xB7
14	270K +/- 1%	2.395V	2.408V	2.421V	0xB8 - 0xBF
15	330K +/- 1%	2.521V	2.533V	2.544V	0xC0 - 0xC9
16	430K +/- 1%	2.667V	2.677V	2.687V	0xCA - 0xD4
17	560K +/- 1%	2.791V	2.800V	2.808V	0xD5 - 0xDD
18	750K +/- 1%	2.905V	2.912V	2.919V	0xDE - 0xFF
19	NC	3.000V	3.300V	3.300V	0xF1 - 0xFF

BOARD ID Table

Board ID	
0	Raven EVT UMA
1	Raven EVT DIS
2	Raven DVT1 UMA
3	Raven DVT1 DIS
4	Raven DVT2 UMA
5	Raven DVT2 DIS
6	Raven Pilot UMA
7	Raven Pilot DIS
8	
9	
10	
11	
12	
13	
14	
15	
16	
17	
18	
19	

SMBUS Control Table

	SOURCE	BATT	Charger	DIMM	Thermal Sensor	FFS	CRT	
EC_SMB_CK1 EC_SMB_DA1	KB9022Q	V	V					
EC_SMB_CK2 EC_SMB_DA2	KB9022Q				V			
EC_I2C_TPCLK EC_I2C_TPDAT	KB9022Q							
APU_SCLK0 APU_SDAT0	APU			V				
APU_SCLK1 APU_SDAT1	APU					V	V	
APU_SIC APU_SID	APU				V			

PCI EXPRESS(GFX)	
Lane 1	PEG (AMD)M2-50
Lane 2	PEG (AMD)M2-50
Lane 3	PEG (AMD)M2-50
Lane 4	PEG (AMD)M2-50
Lane 5	RV2 NA
Lane 6	RV2 NA
Lane 7	RV2 NA
Lane 8	RV2 NA

CLOCK SIGNAL	
CLKOUT_PCIE0	dGPU
CLKOUT_PCIE1	10/100 LAN(GIGA RESERVE)
CLKOUT_PCIE2	NGFF Card (WLAN)
CLKOUT_PCIE3	NVME SSD

Symbol Note :

 : means Digital Ground

 : means Analog Ground

Voltage Rails

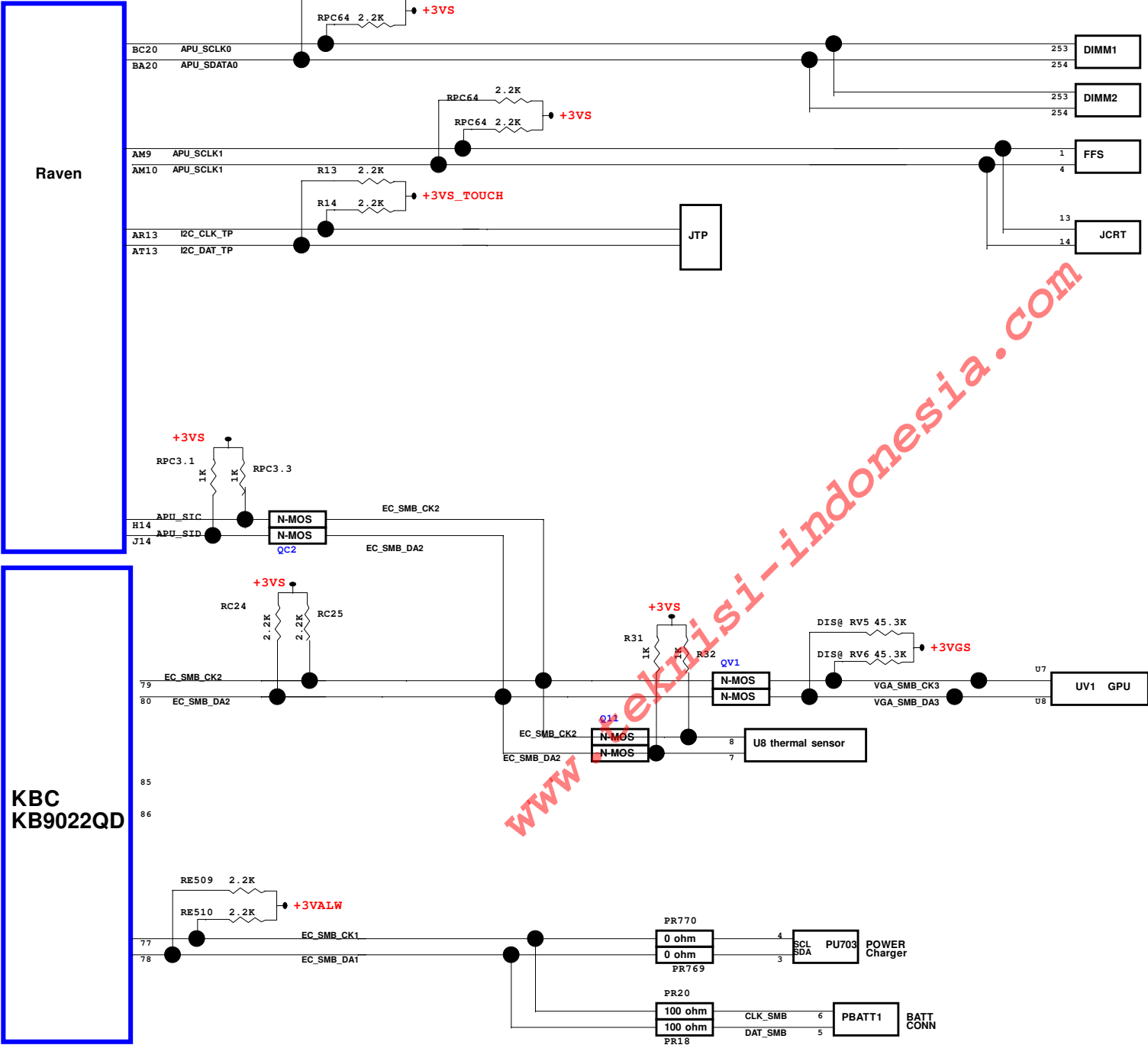
Power Plane	Description	S0	S3	S4/S5
+SDC_IN	Adapter power supply	N/A	N/A	N/A
+17.4V_BATT++	Bat try power supply	N/A	N/A	N/A
+19VB	AC or DC for power circuit	N/A	N/A	N/A
+APU_VDDCORE	Core voltage for APU	ON	OFF	OFF
+APU_VDDSOC	VDDSOC voltage for APU	ON	OFF	OFF
+3VALW_APU	3V always for APU	ON	ON	ON*
+0.8VALW_APU	0.8V always for APU	ON	ON	ON*
+1.8V_ALW_APU	1.8V always for APU	ON	ON	ON*
+0.8VS	0.8V sustain for APU	ON	OFF	OFF
+VGA_CORE	VGA core power rail for GPU	ON	OFF	OFF
+1.35V_MEM_GFX	+1.35VS power rail for GPU and VRAM	ON	OFF	OFF
+3VGS	+3VS power rail for GPU	ON	OFF	OFF
+1.8VGS	+1.8VS power rail for GPU	ON	OFF	OFF
+0.95VSDGPU	0.95V power rail for GPU	ON	OFF	OFF
+3.3V_VDD_PIC	3.3V power rail for PD chip	ON	OFF	ON*
+3VALW	System +3VALW always on power rail	ON	ON	ON*
+3VLP	+19VB to +3VLP power rail for suspend power	ON	ON	ON
+3VS	System +3VS power rail	ON	OFF	OFF
+0.6V_DDR_VTT	DDR +0.6VS power rail for DDR terminator	ON	OFF	OFF
+1.2V_DDR	DDR4/L-RS +1.2V power rail	ON	ON	OFF
+2.5V_MEM	DDR4/L-RS +2.5V power rail	ON	ON	OFF
+1.8VS	System +1.8VS power rail	ON	OFF	OFF
+5VALW	System +5VALW power rail	ON	ON	ON*
+5VS	System +5VS power rail	ON	OFF	OFF
+RTCVCC	RTC power	ON	ON	ON

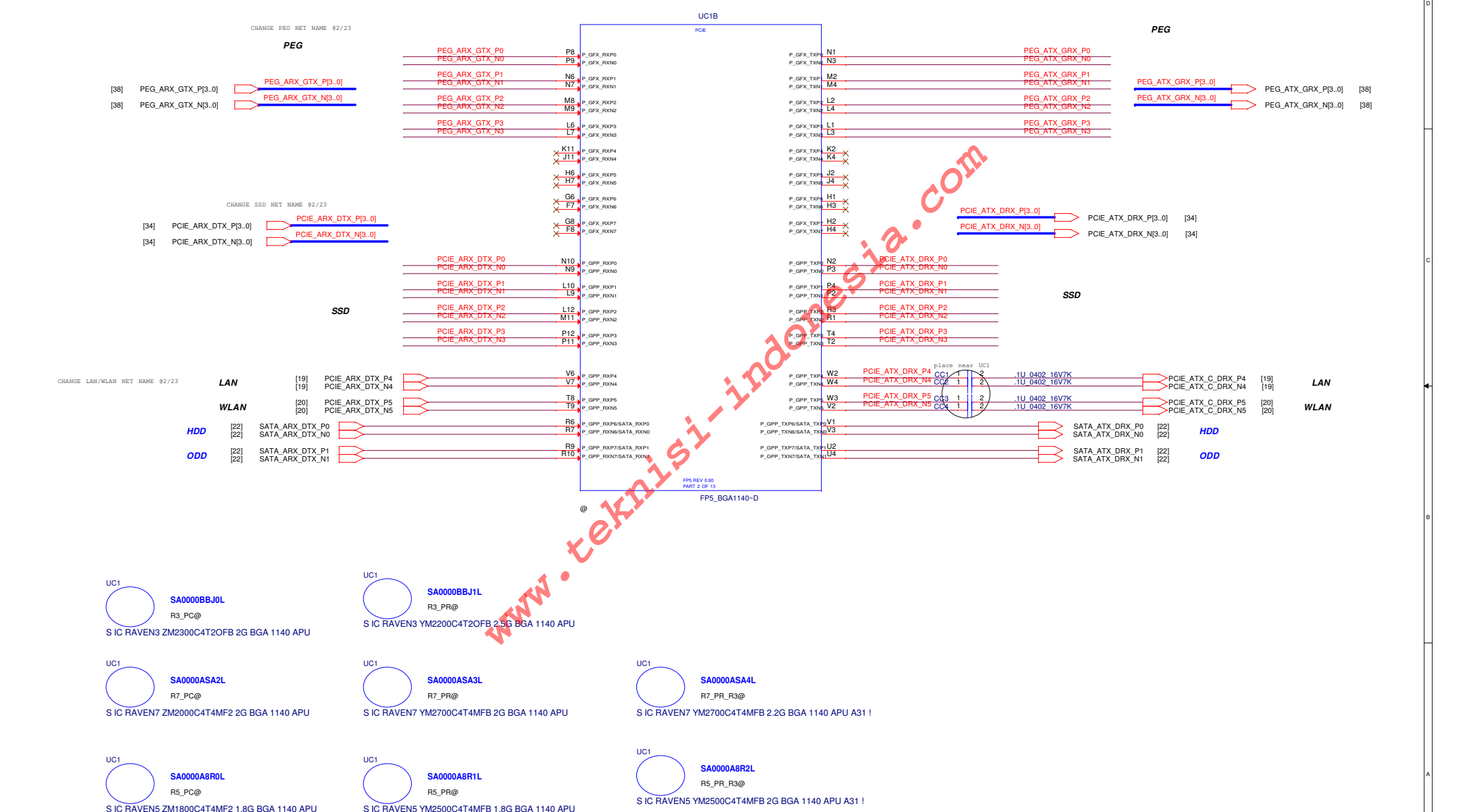
Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF

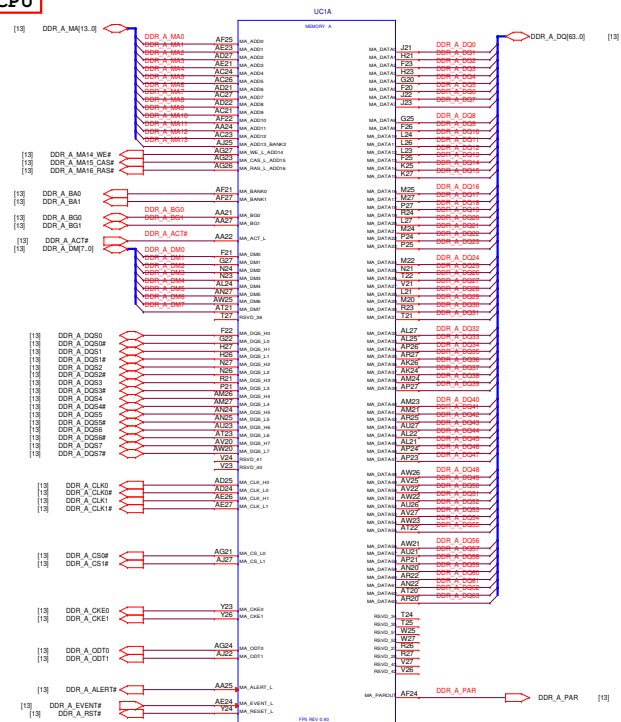
USB3.0	
0_Port0	TYPE C
0_Port1	USB3 connector 1
0_Port2	USB3 connector 2
0_Port3	progaming DP signal
1_Port0	
1_Port1	
USB2.0	
0_Port0	TYPE C
0_Port1	USB connector 1
0_Port2	USB connector 2
0_Port3	Camera
1_Port0	USB connector 1(D/B)
1_Port1	USB HUB
PCI EXPRESS(GPP)	
Lane 1	NVME SSD
Lane 2	NVME SSD
Lane 3	NVME SSD
Lane 4	NVME SSD
Lane 5	10/100 LAN(GIGA RESERVE)
Lane 6	NGFF Card (WLAN)
Lane 7	use sata interface
Lane 8	use sata interface
SATA	
SATA0	HDD
SATA1	ODD

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SMBus Block Diagram







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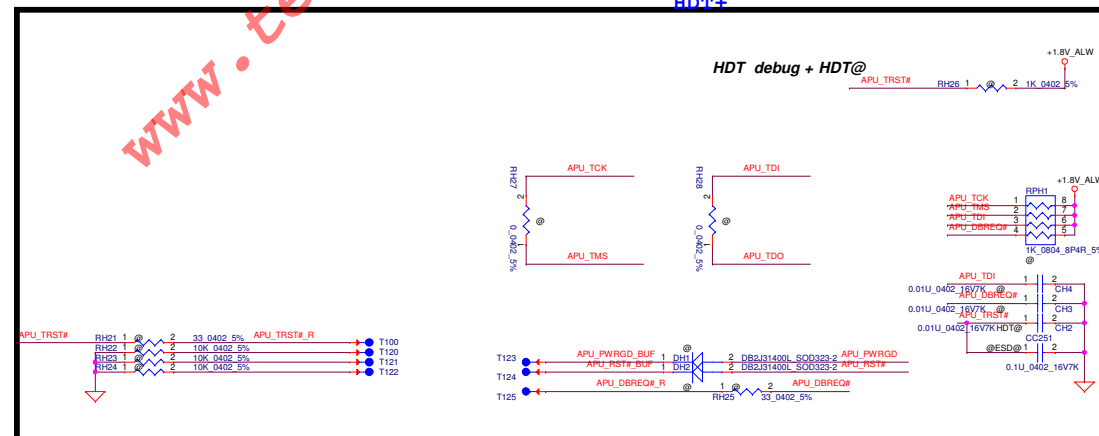
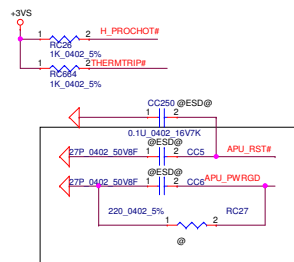
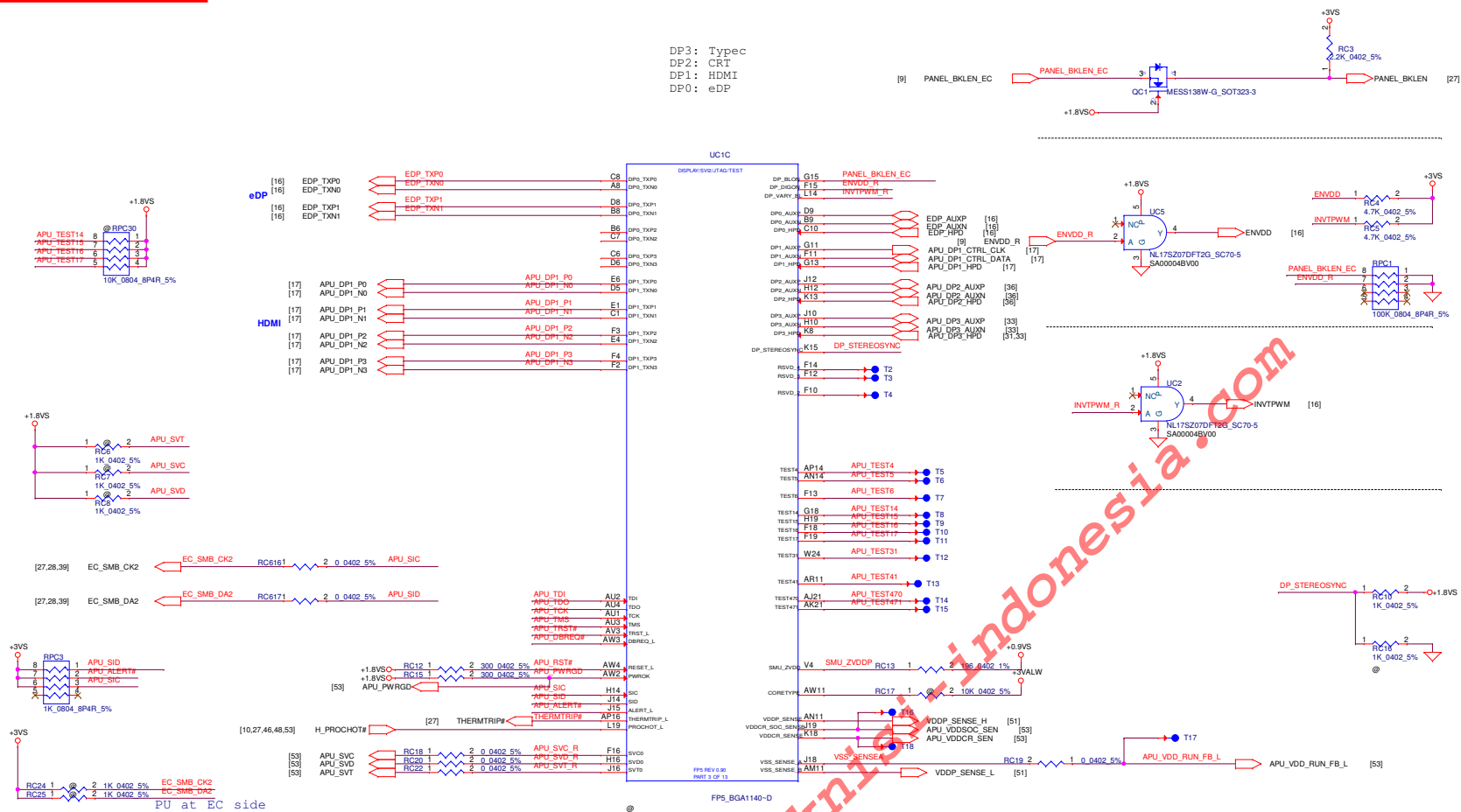


EVENT# pull high

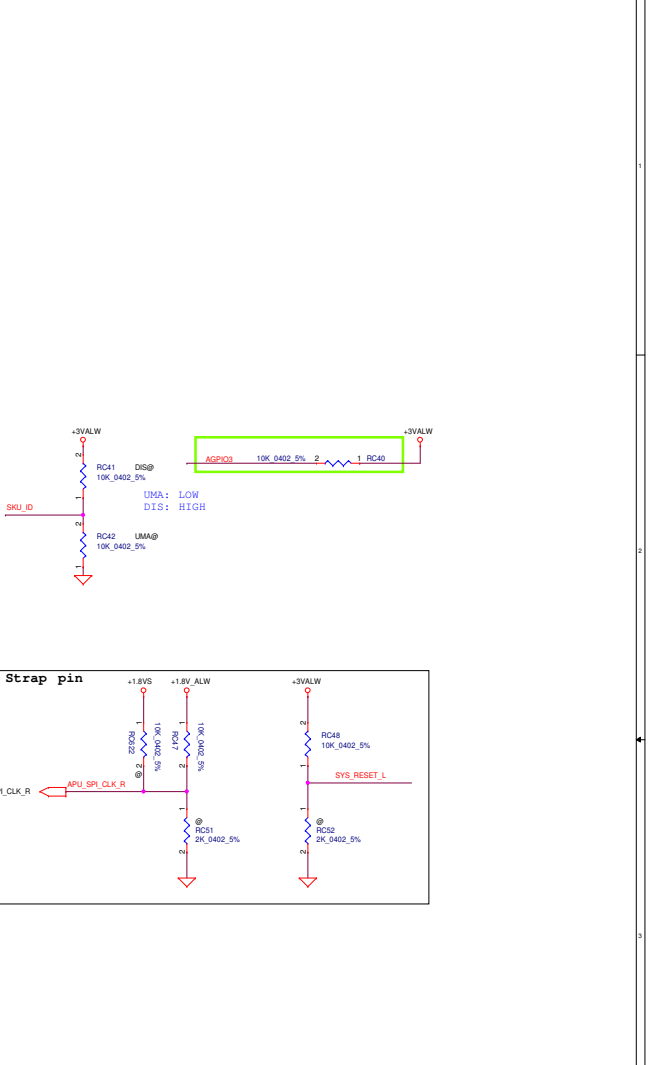


Main Func = CPU

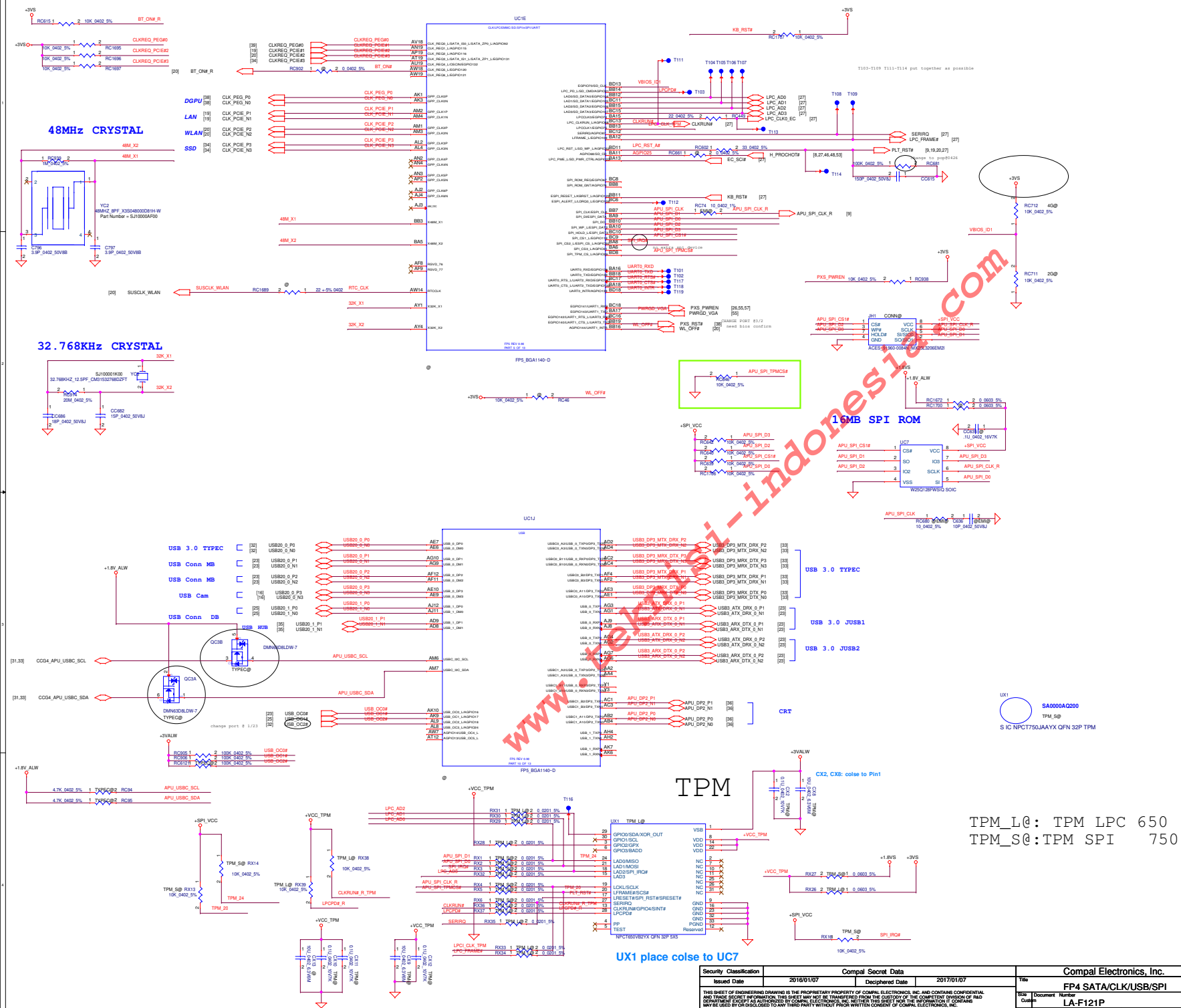
```
DP3: Typec
DP2: CRT
DP1: HDMI
DP0: eDP
```



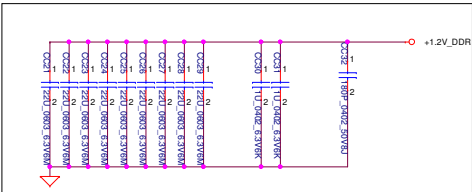
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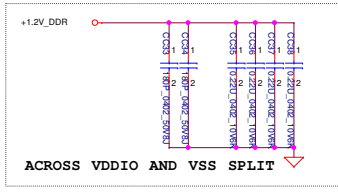
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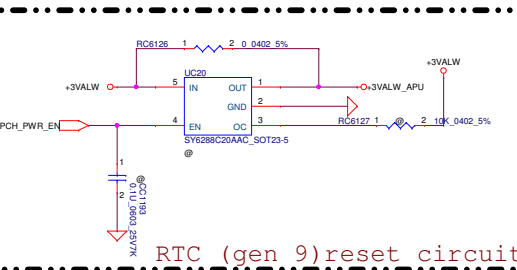
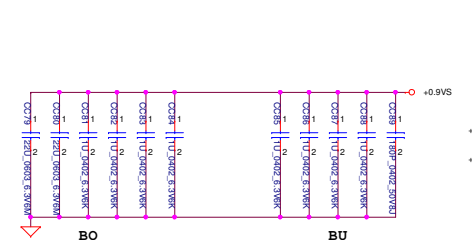
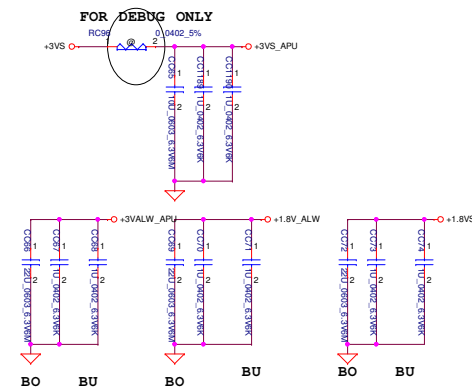
Main Func = CPU



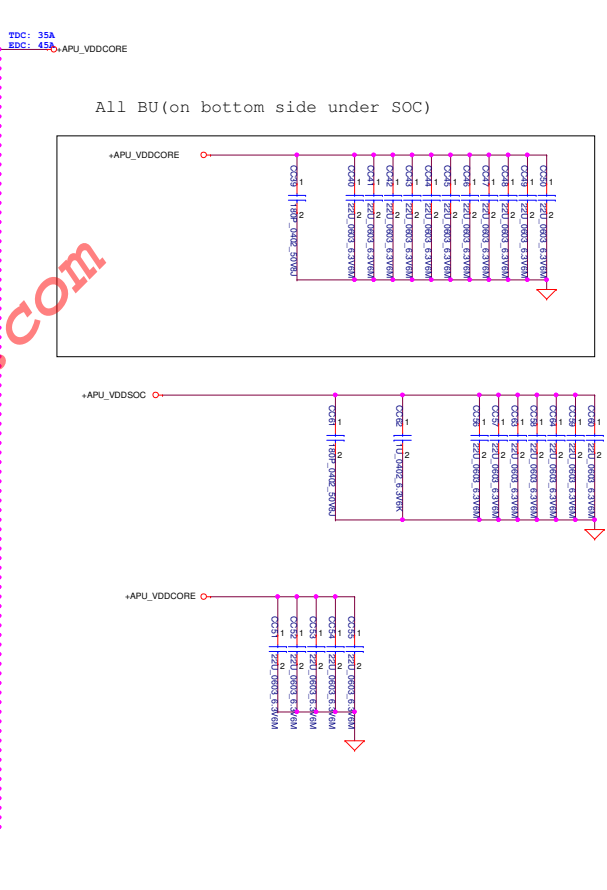
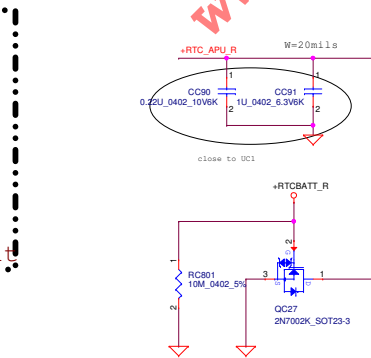
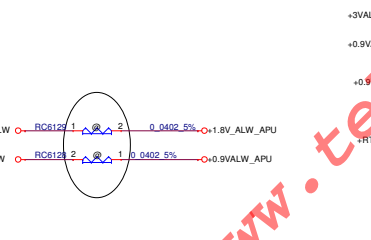
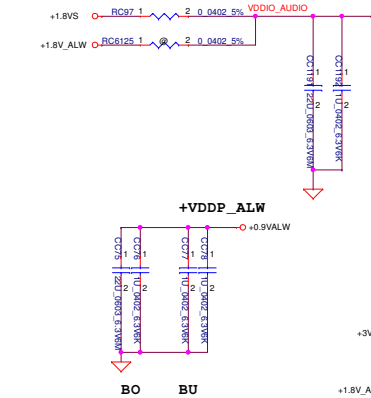
All BU(on bottom side under SOC)



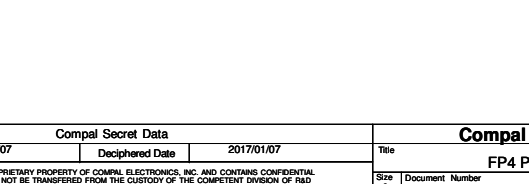
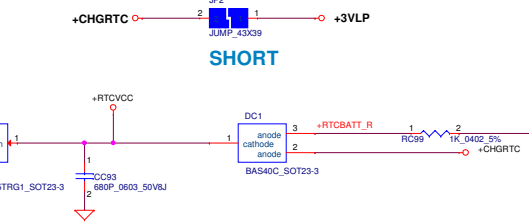
ACROSS VDDIO AND VSS SPLIT



RTC (gen 9)reset circuit



All BU(on bottom side under SOC)



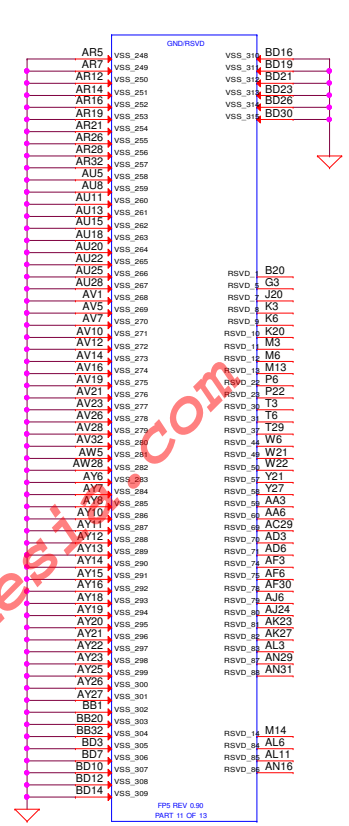
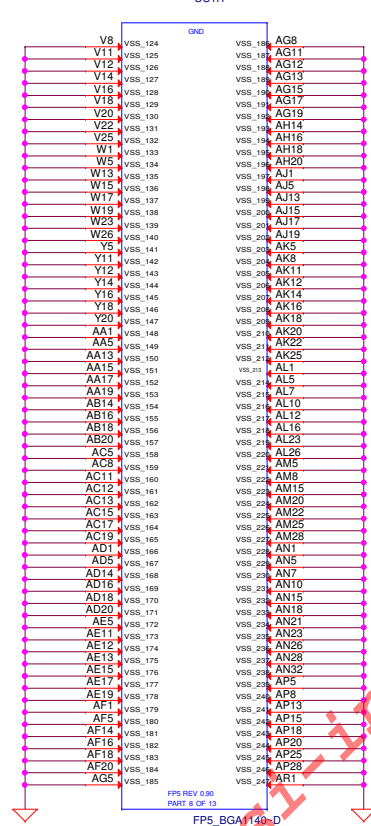
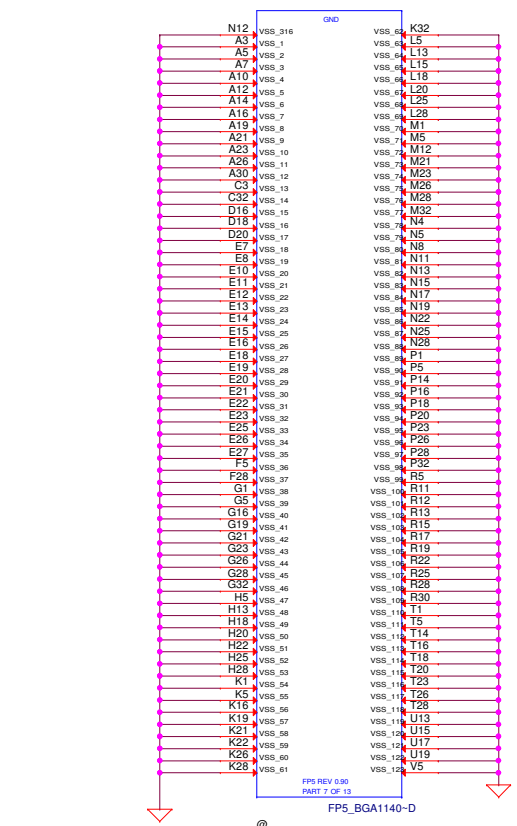
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Main Func = CPU

UC1G

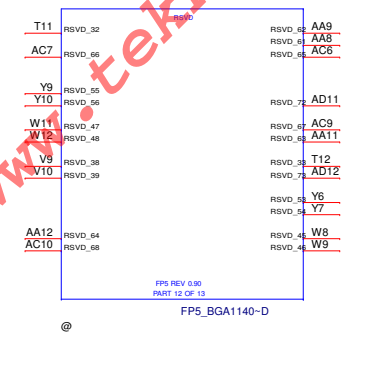
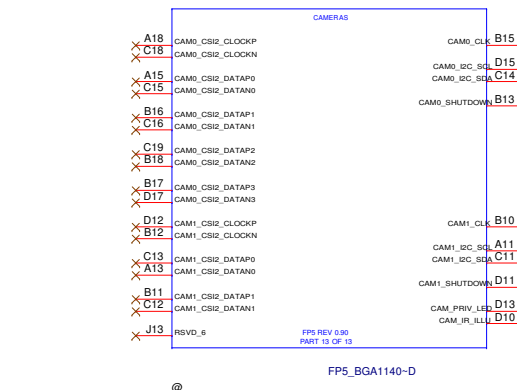
UC1H

UC1K



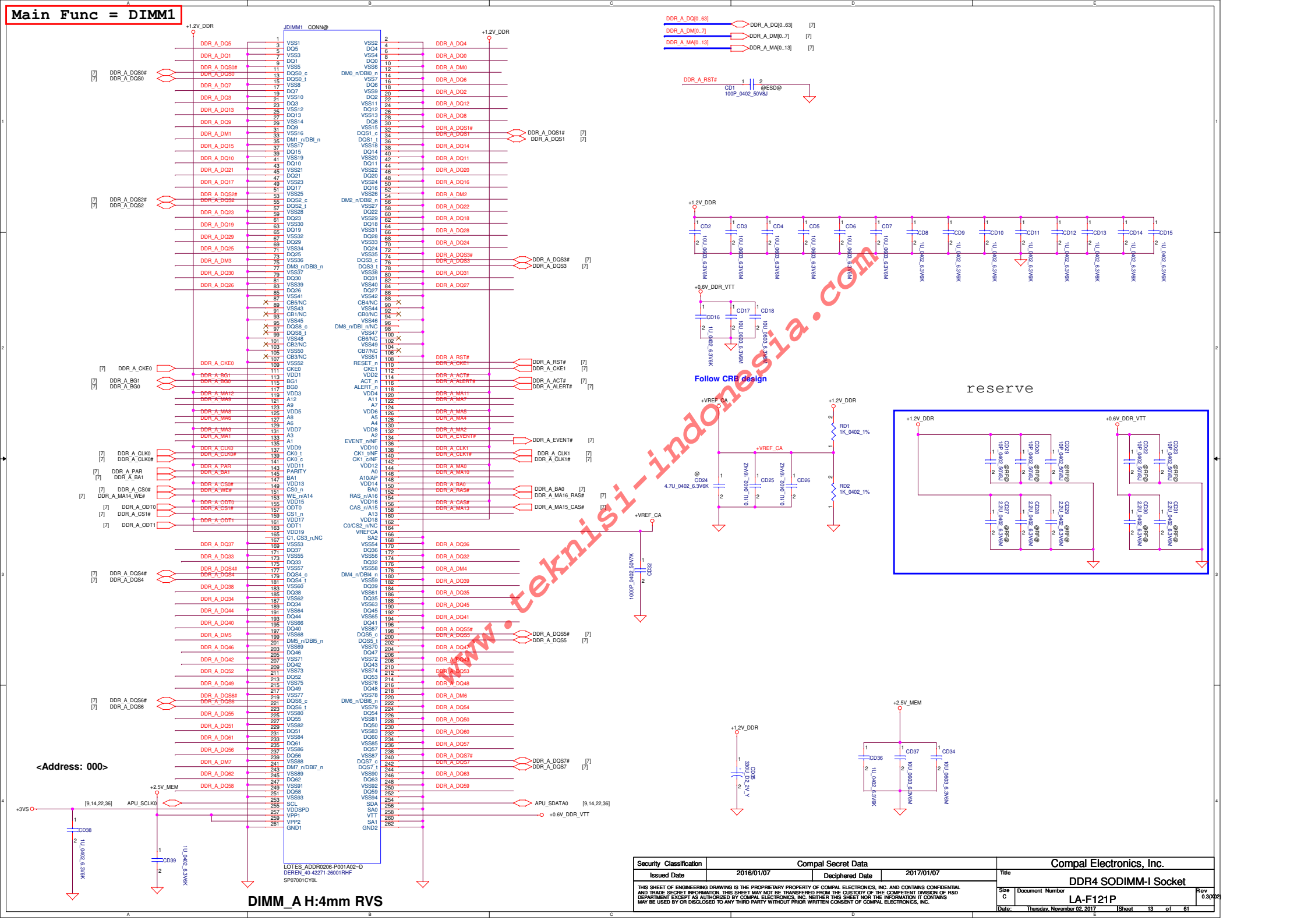
UC1M

UC1L

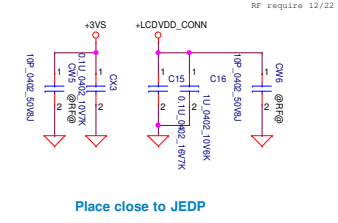
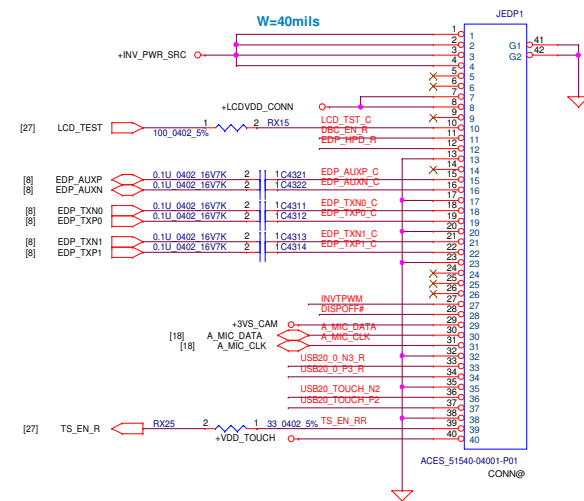
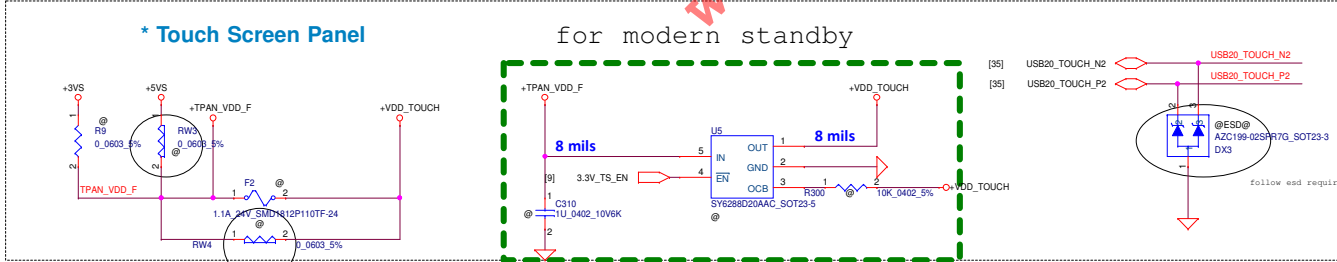
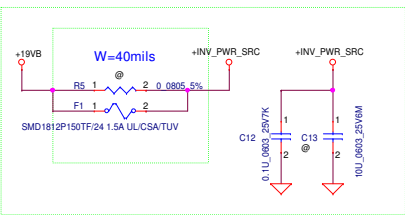
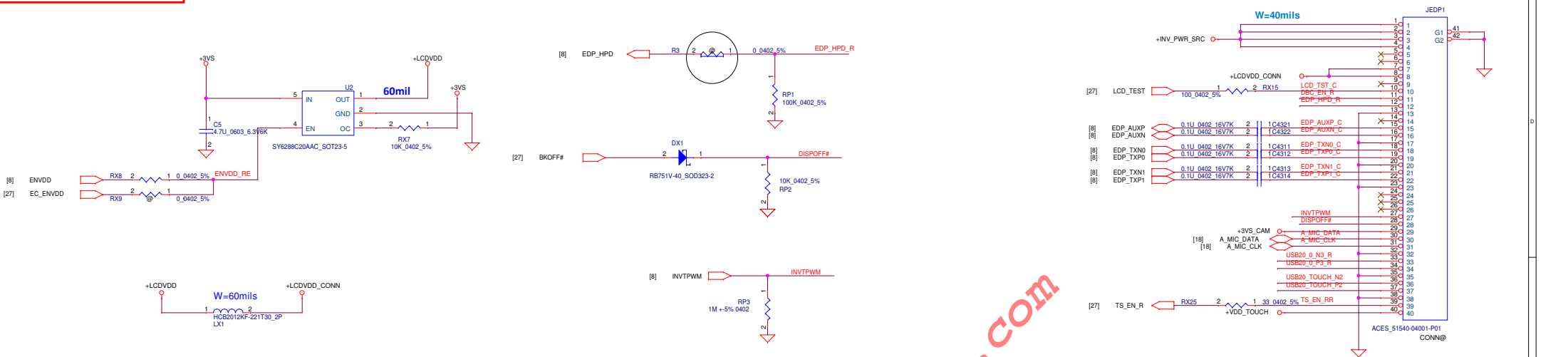


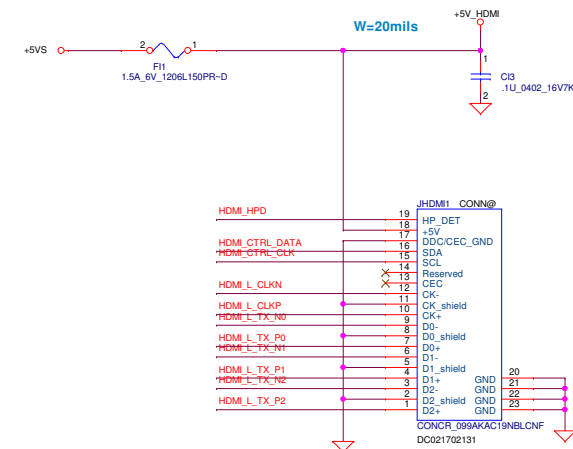
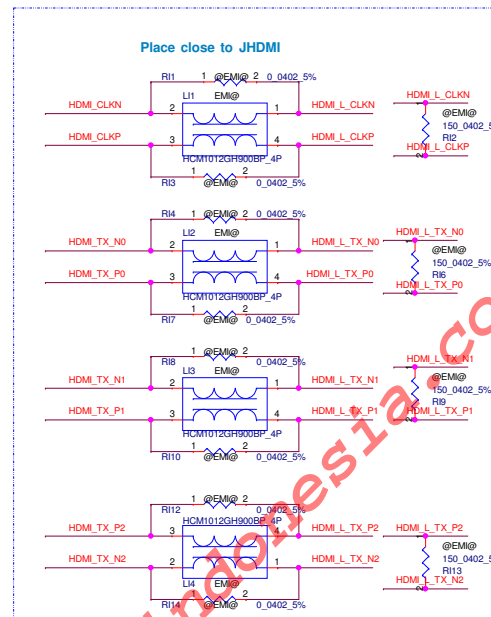
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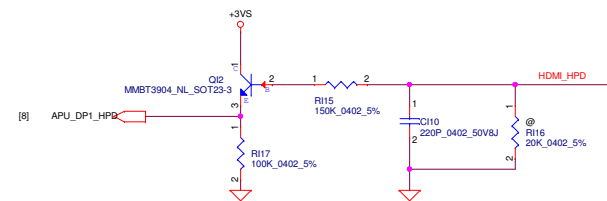
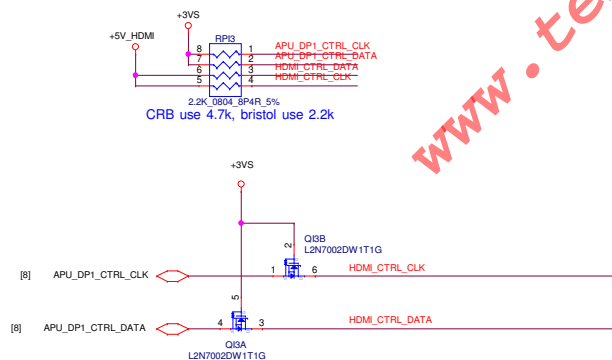


Main Func = LCD

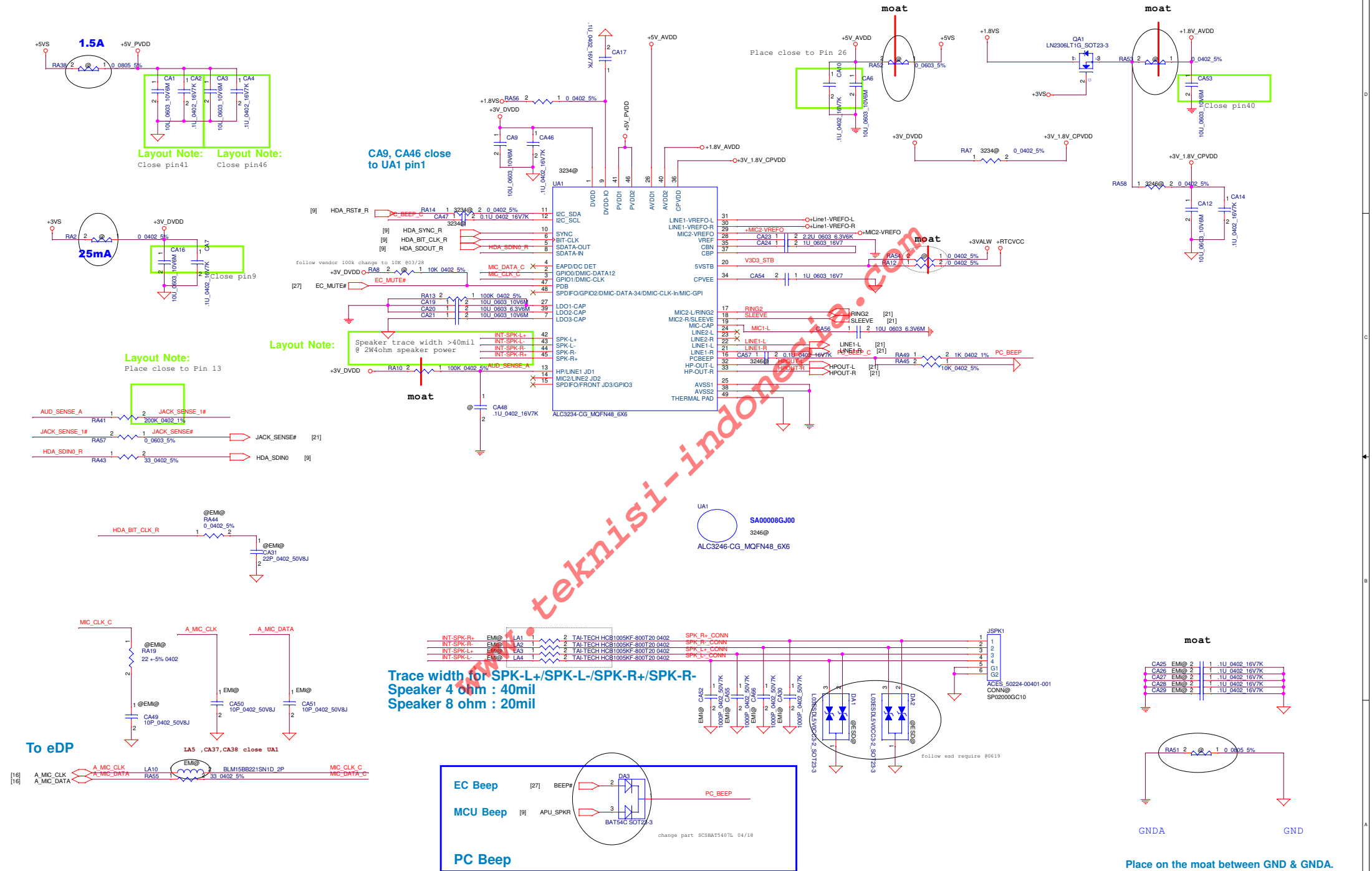




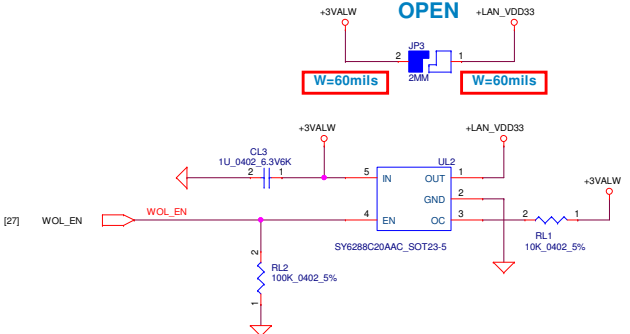
45@ ROYALTY HDMI W/LOGO	
Part Number	Description
RO0000002HM	HDMI W/Logo:RO0000002HM



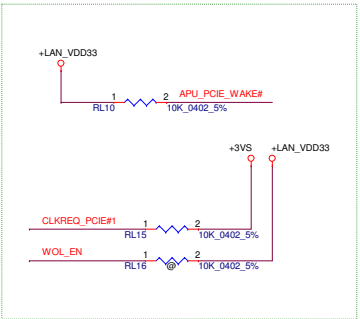
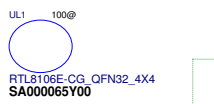
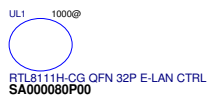
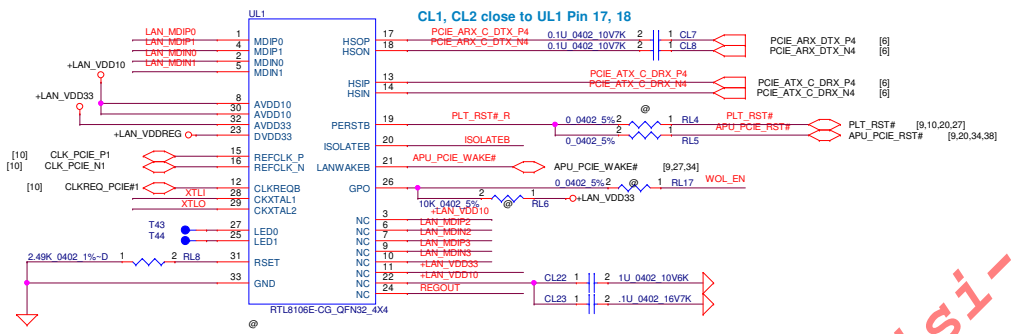
Main Func = Audio



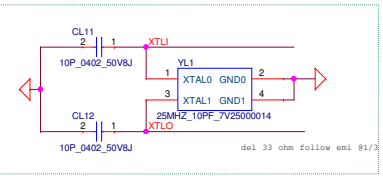
+LAN_VDD33 rising time(10%~90%) : >0.5ms and <100ms



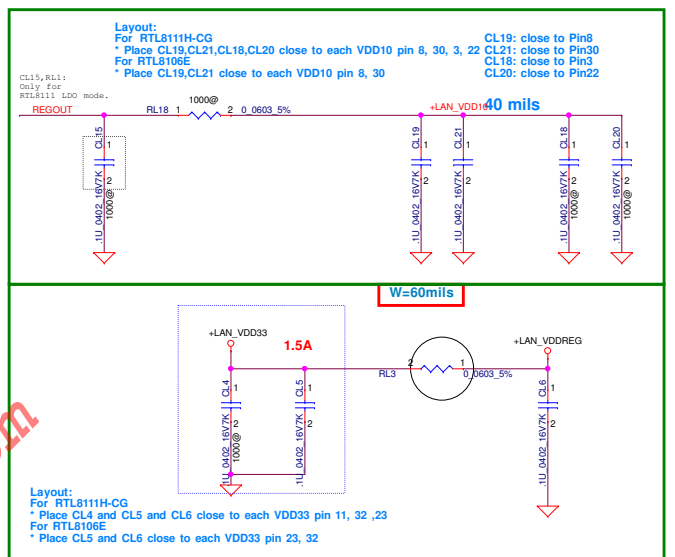
LAN power Noise +LAN_VDD33 < 200mV Vpeak to Vpeak.
LAN power Noise +LAN_VDD10 < 100mV Vpeak to Vpeak.



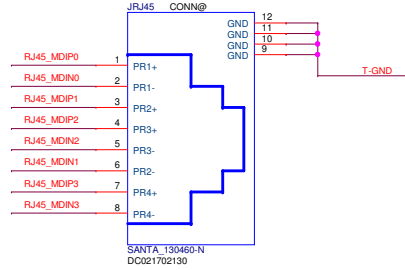
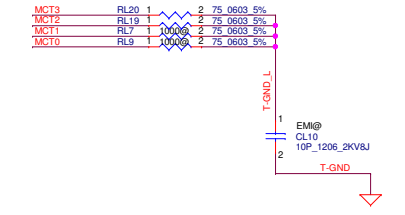
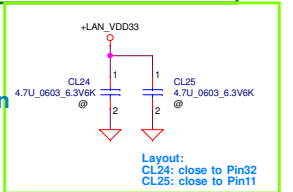
Reserve 10K pull LAN_IO



XTAL

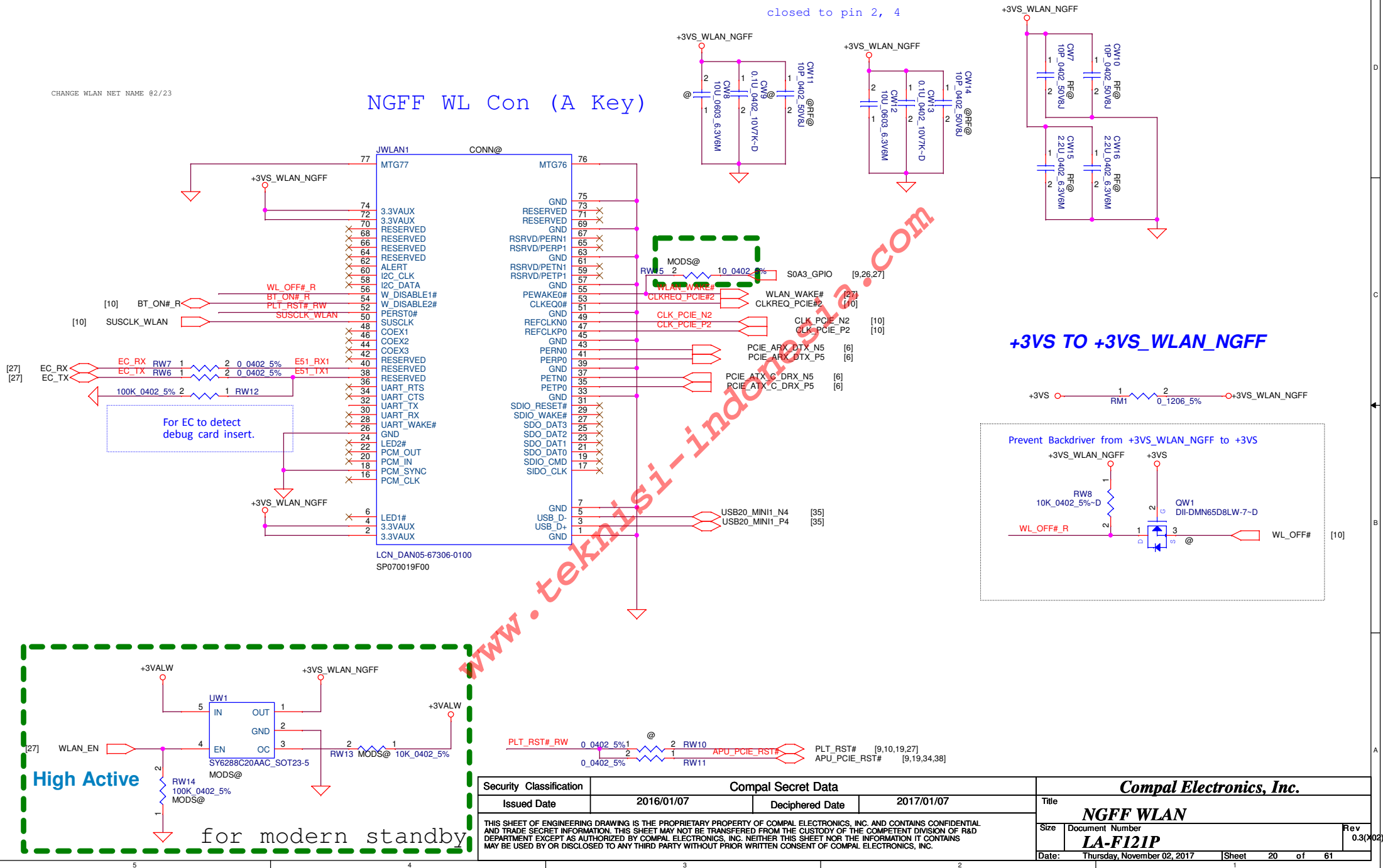


Place close to TCT pin

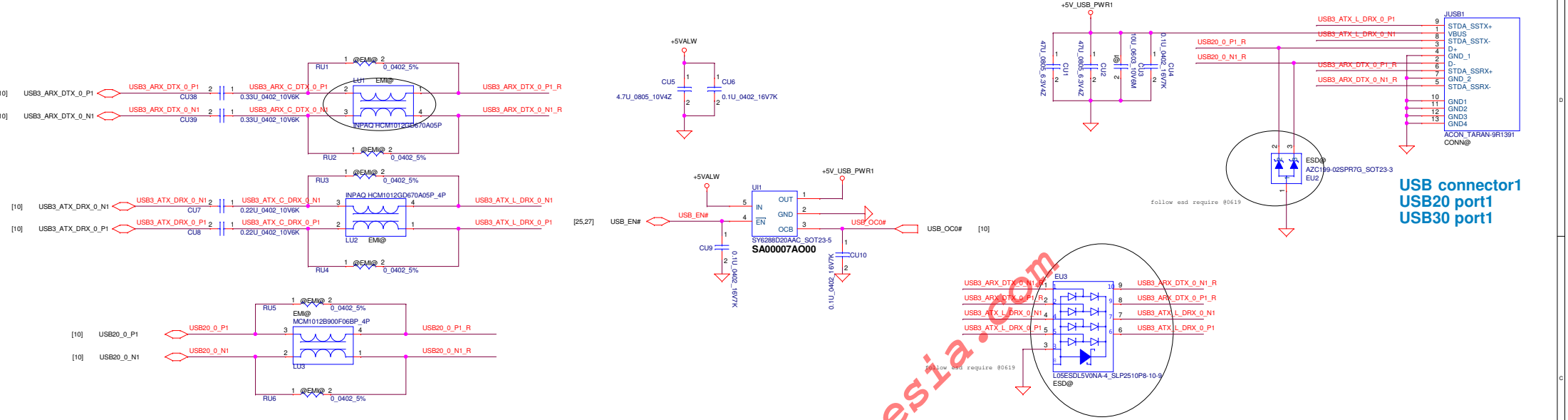


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Size	Custom	Document Number	LA-F121P	Rev 0.3(2016)
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Main Func = WLAN



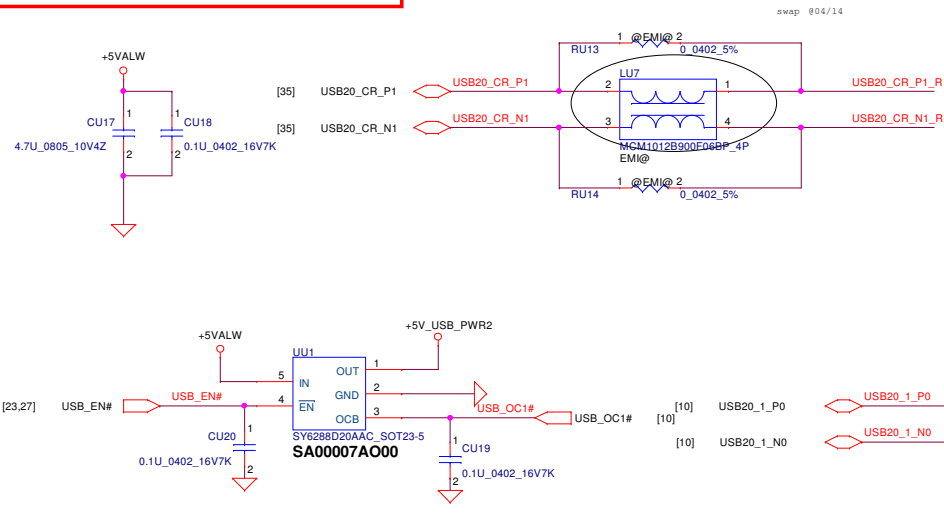
Main Func = USB3.0 Port1



Main Func = USB3.0 Port2

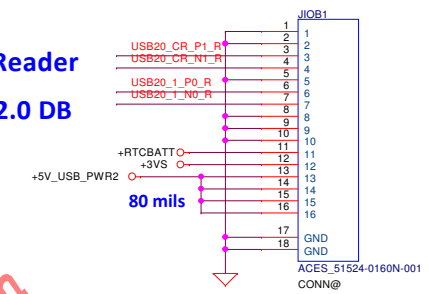


Main Func = IO Connector



I/O Board Connector

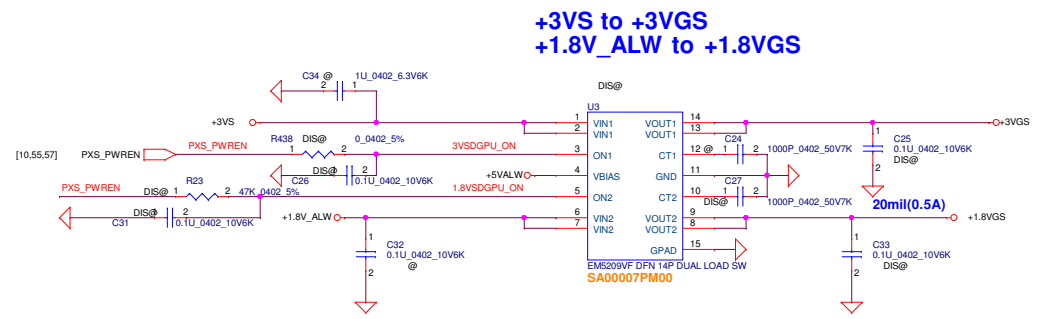
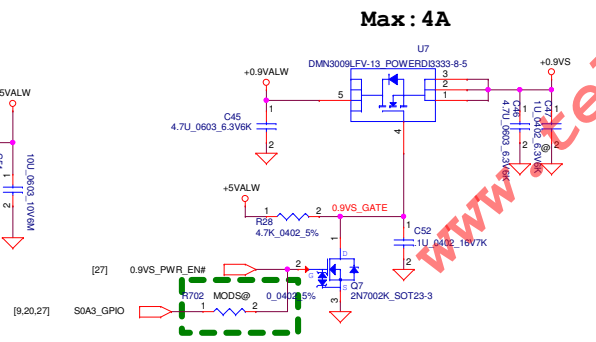
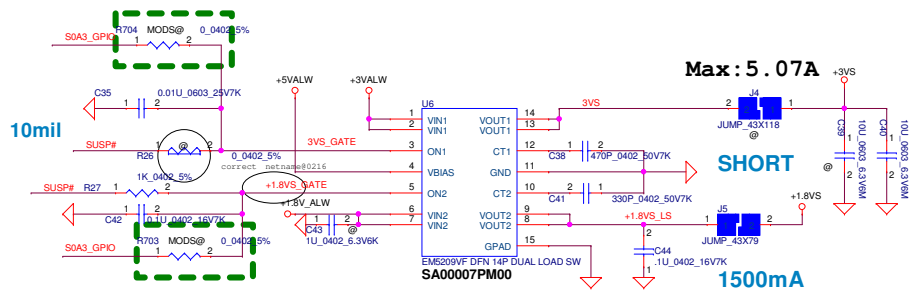
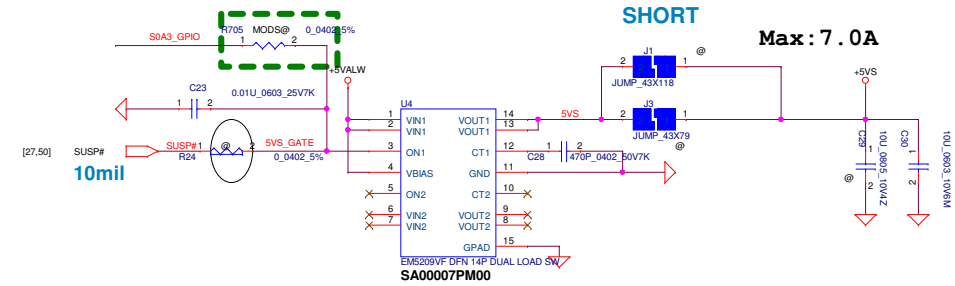
CardReader
USB2.0 DB

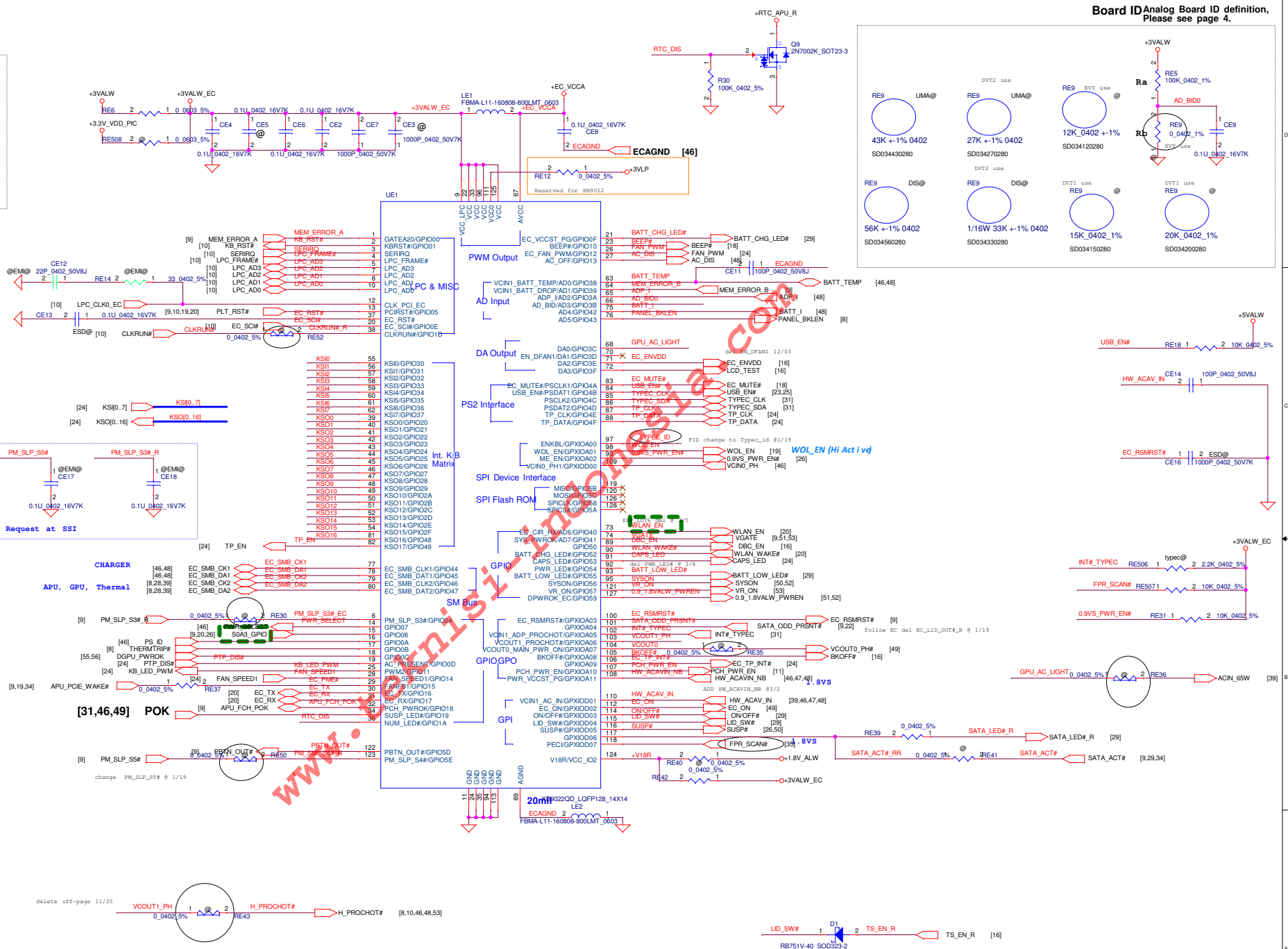
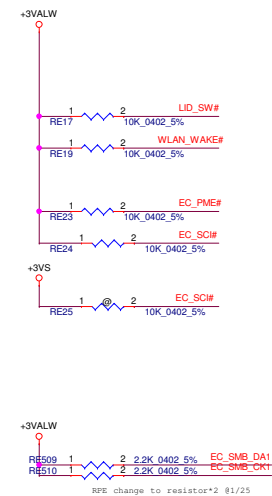
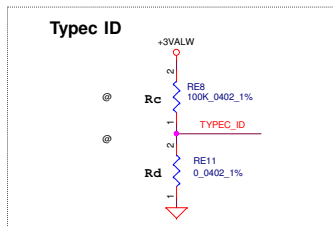


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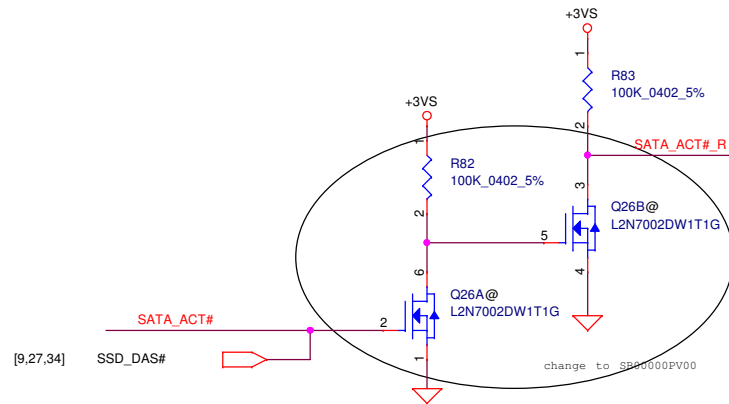
+5VS and +3VS switch



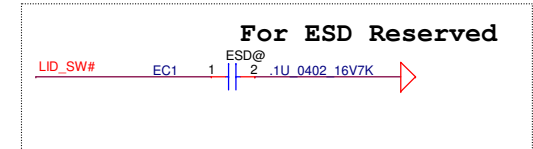
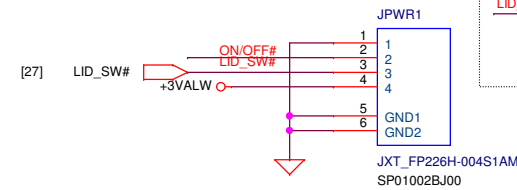


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				Date:	Thursday, November 02, 2017	Sheet 27 of 61

Main Func = POWER BTN



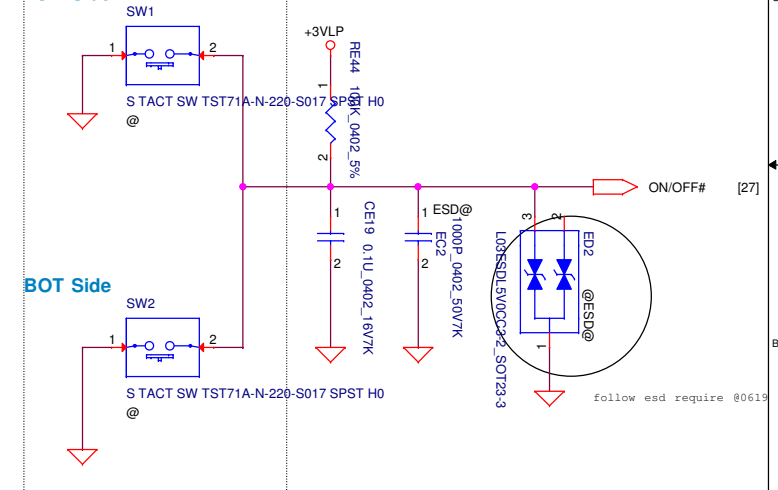
Power button



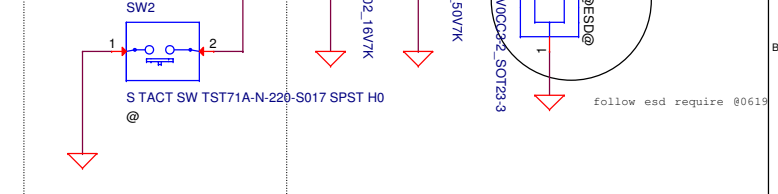
Pop only before MP

ON/OFF switch

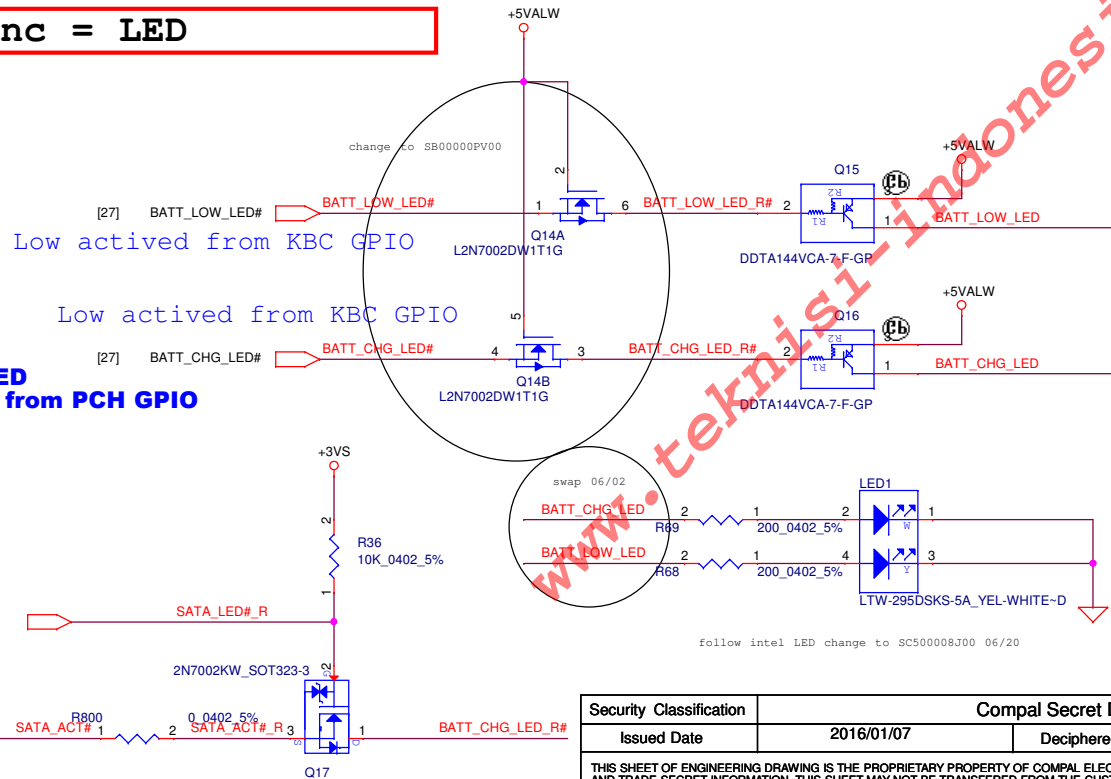
TOP Side



BOT Side



Main Func = LED



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ZZZ

Part Number	Description
DAZ21O00100	PCB CAL51 LA-F121P LS-F114P/F121P/F122P

PCB_R1@

ZZZ1

Part Number	Description
DAZ21O00101	PCB CAL51 LA-F121P LS-F114P/F121P/F122P GOLD A31

PCB_R3G@

ZZZ2

Part Number	Description
DAZ21O00102	PCB CAL51 LA-F121P LS-F114P/F121P/F122P TRIPOD A31

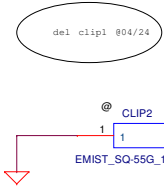
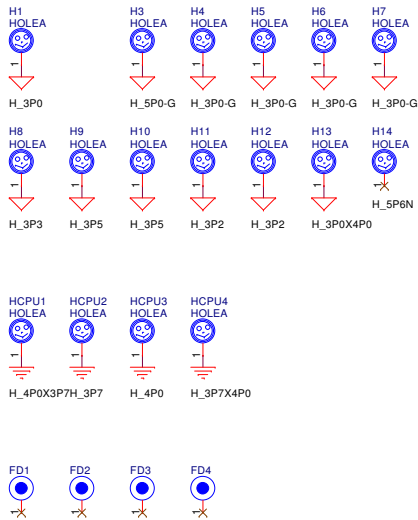
PCB_R3T@

ZZZ3

Part Number	Description
DAZ21O00104	PCB CAL51 LA-F121P LS-F114P/F121P/F122P T-MAC A31

PCB_R3H@

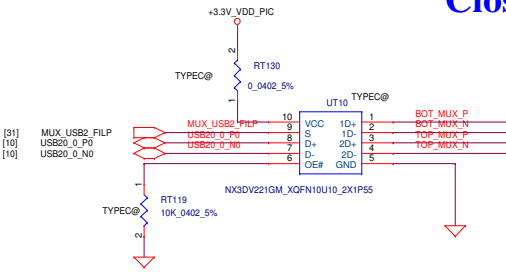
Screw hole/FD



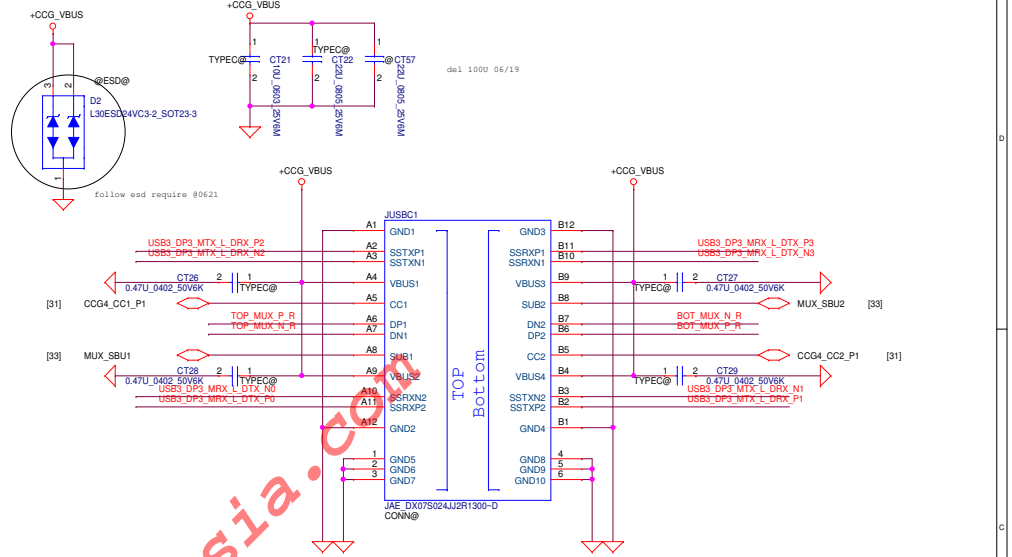
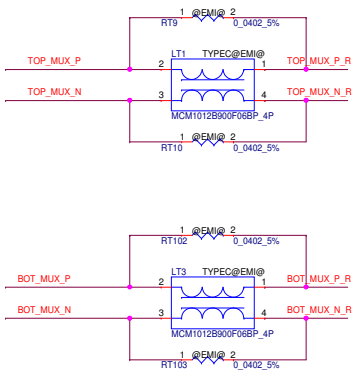
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Main Func = USB2 Mux

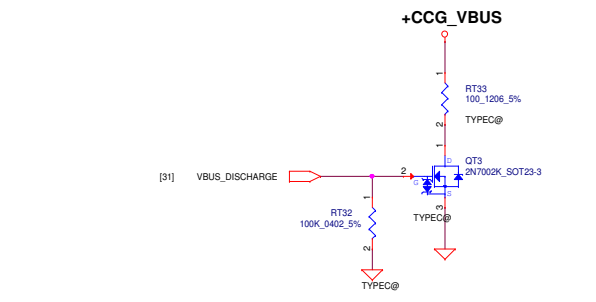
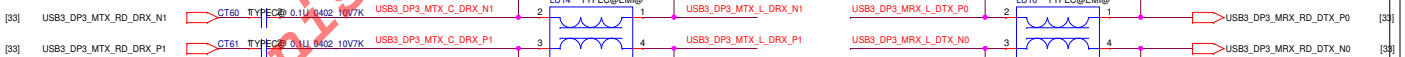
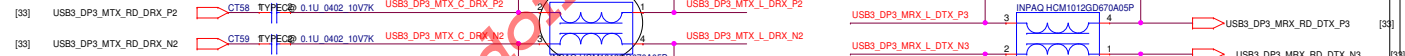
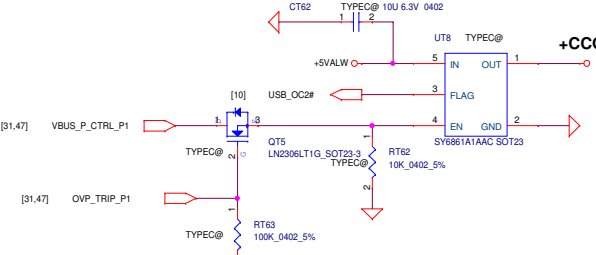
Close to JUSBC1 <500mil



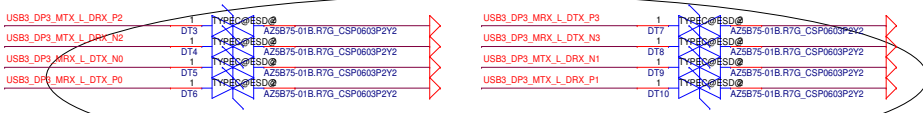
S	OE#	OUT PUT
Low	Low	1D+/1D-
High	Low	2D+/2D-



5V@3A

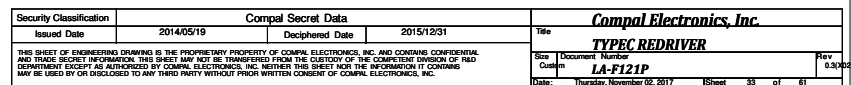


change footprint 06/19



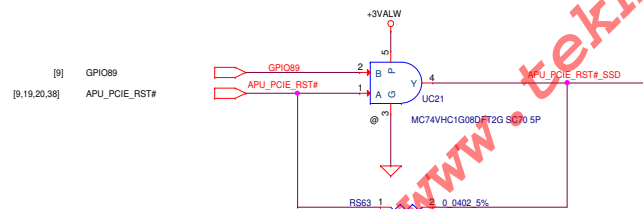
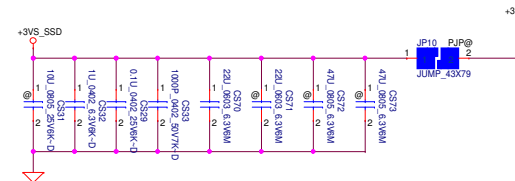
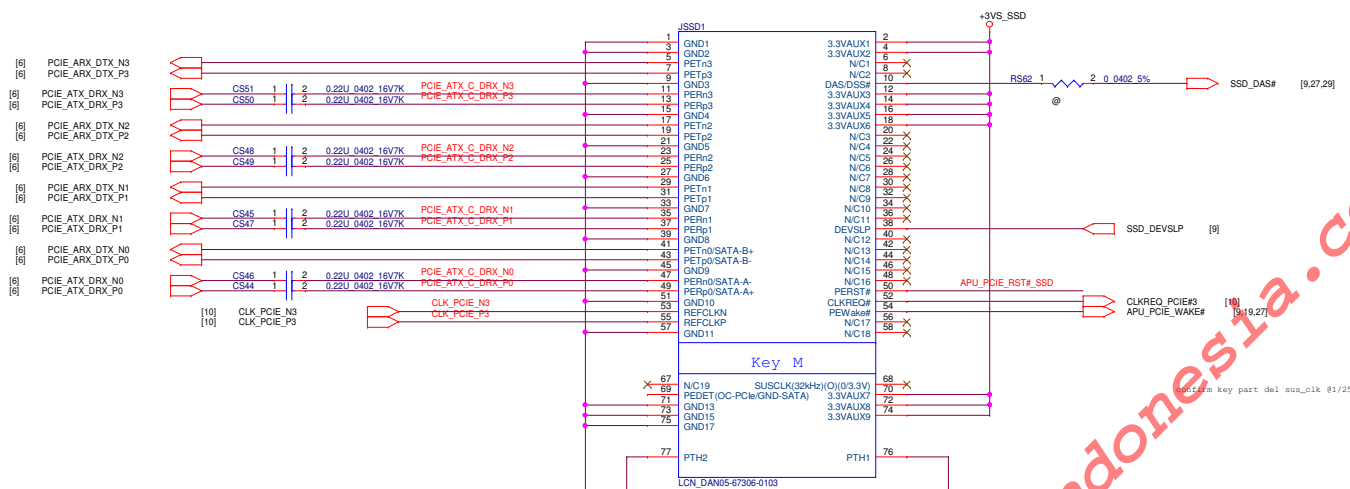
Type-C 5V Provide Path Control

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[illegible]

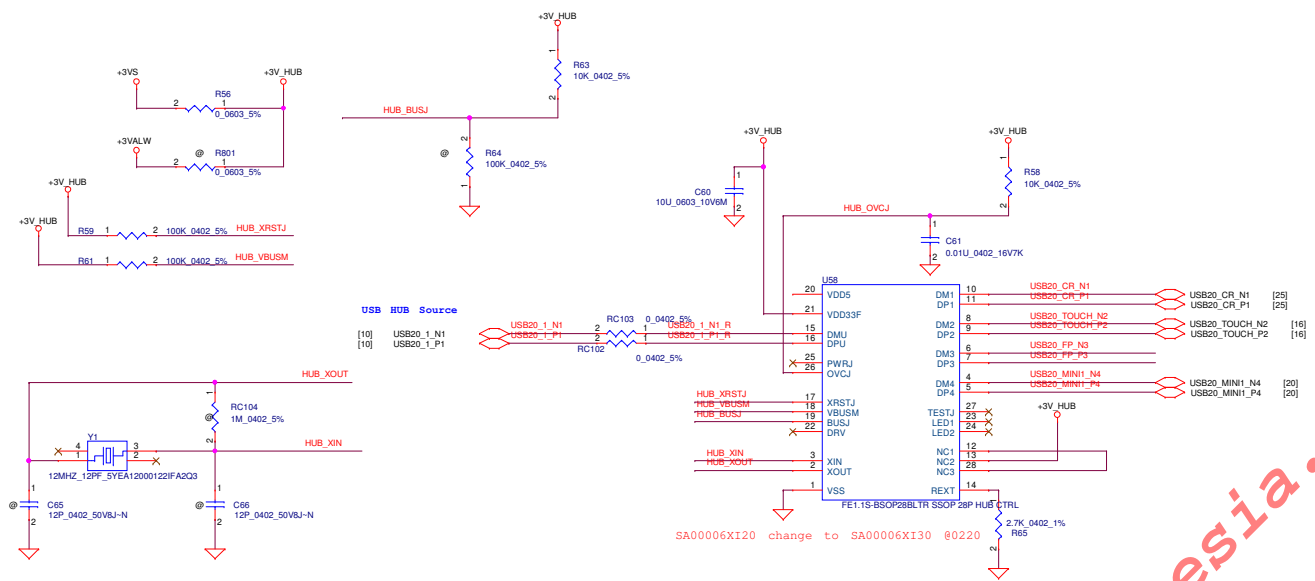
Main Func = SSD

NGFF Key M

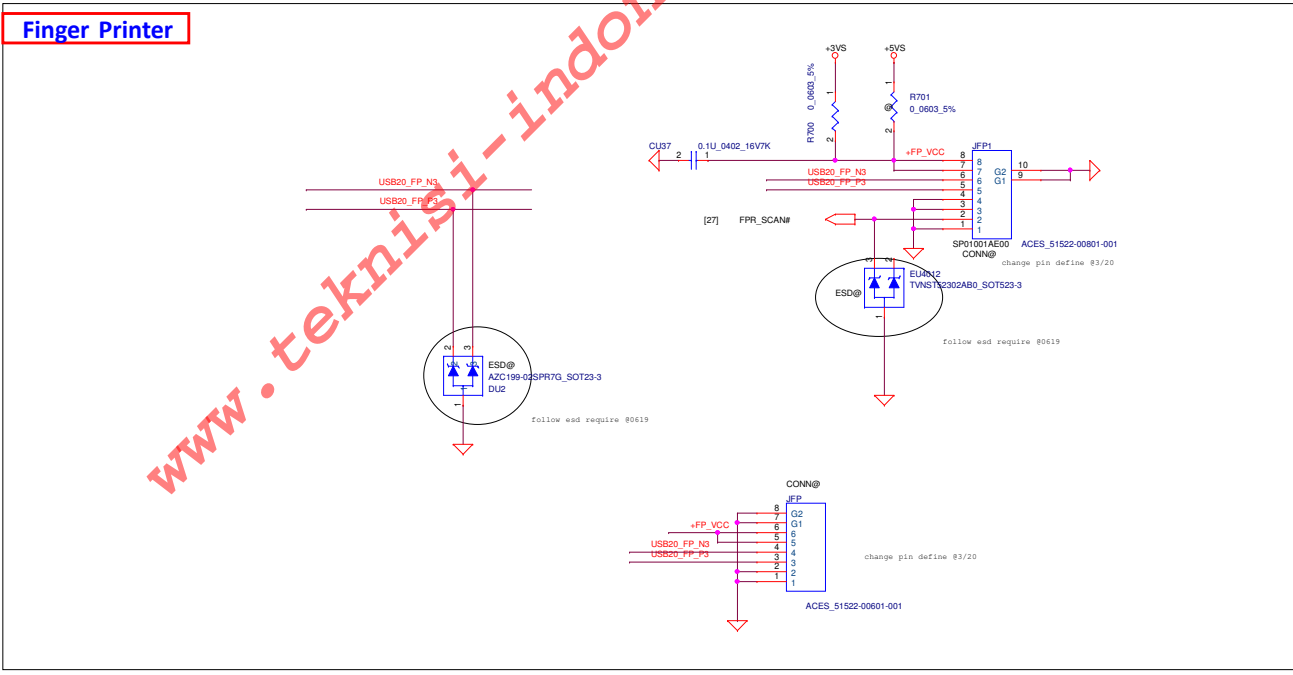


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Main Func = USB HUB

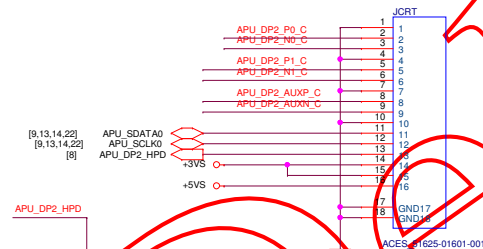


Finger Printer

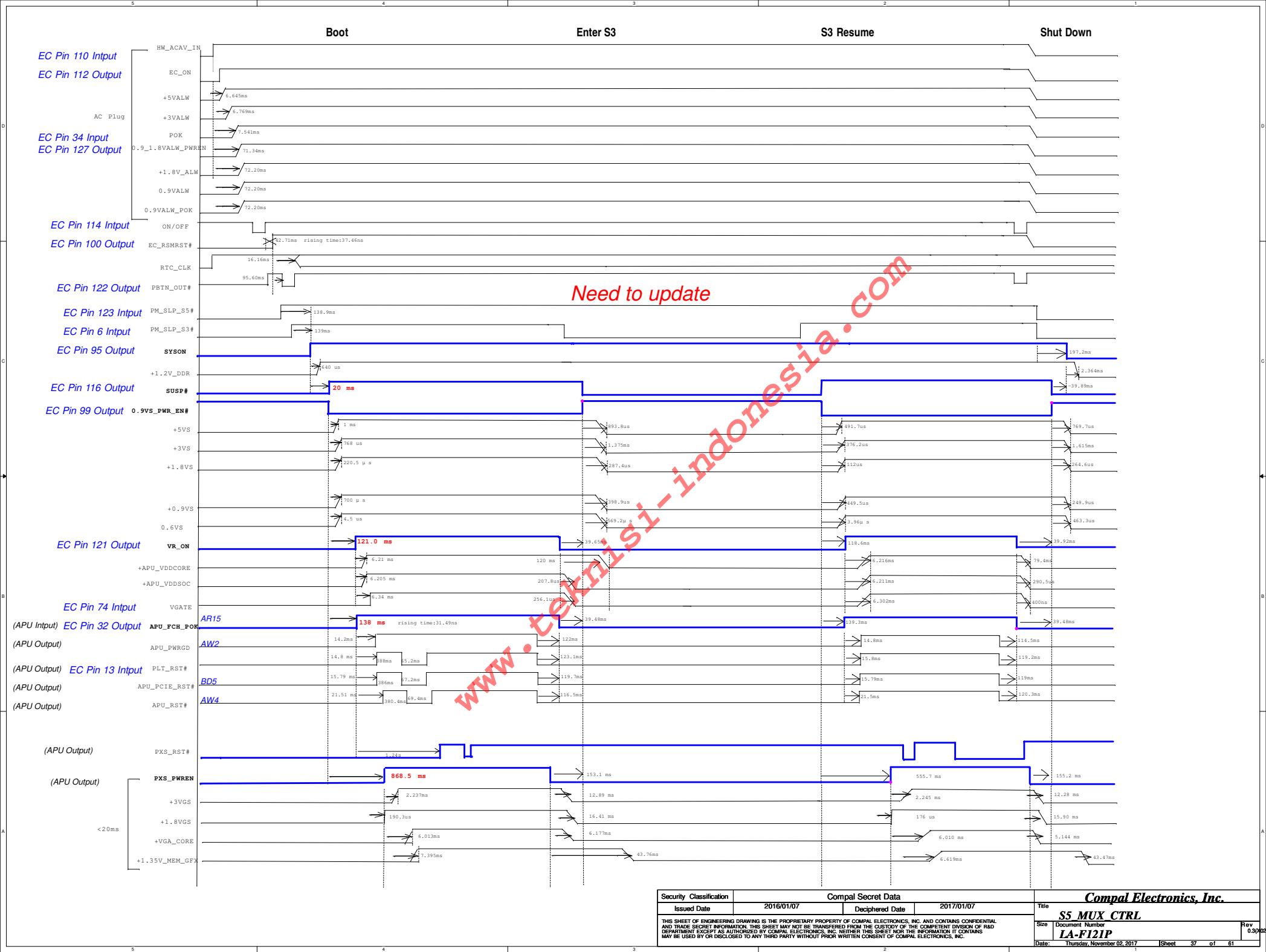


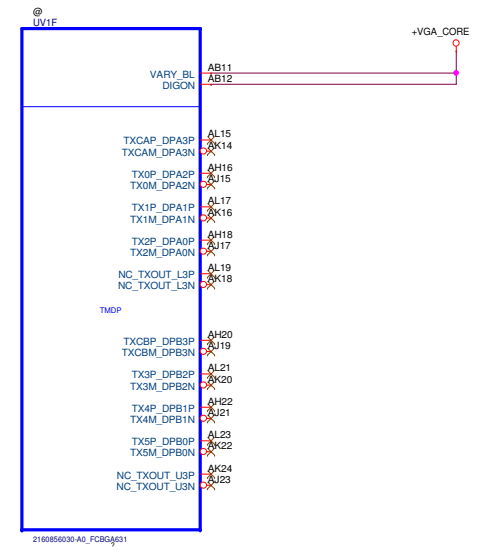
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Issued Date	2014/05/19	Deciphered Date	2015/12/31	Title	USB HUB
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CRT



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GPU R3

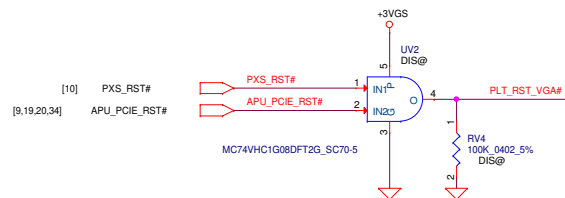
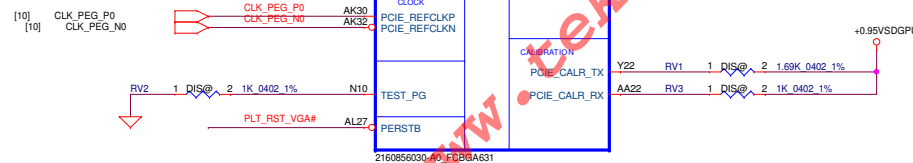
R17M-M2-50



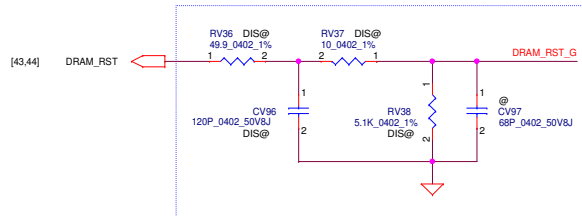
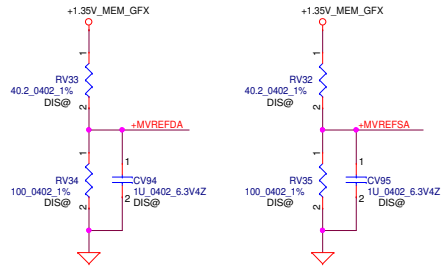
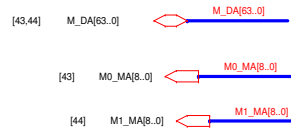
S IC 216-0889004 A0 R17M-M2-50 WESTON XT BGA 631P GPU A31 !



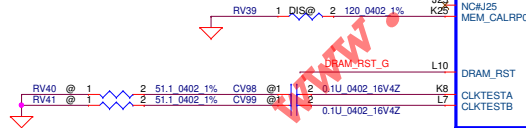
S IC 216-0889004 A0 R17M-M2-50 WESTON XT BGA 631P GPU 0FD



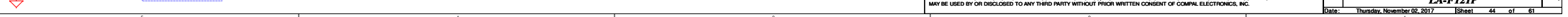
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Issued Date	2016/01/07	Deciphered Date	2017/01/07	Title	M30/M70_PCIE/DP
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Place close to GPU (within 25mm)
and place component within (5mm) close to each other



M0_MA0			M1_MA0		
M0_MA0	K27	Q0A0_0	M0_MA0	K20	Q0A0_0
M0_MA1	J29	Q0A0_1	M0_MA1	H23	Q0A0_1
M0_MA2	H30	Q0A0_2	M0_MA2	G23	Q0A0_2
M0_MA3	H32	Q0A0_3	M0_MA3	G24	Q0A0_3
M0_MA4	G29	Q0A0_4	M0_MA4	H24	Q0A0_4
M0_MA5	F32	Q0A0_5	M0_MA5	J19	Q0A0_5
M0_MA6	F30	Q0A0_6	M0_MA6	K19	Q0A0_6
M0_MA7	C30	Q0A0_7	M0_MA7	G20	Q0A0_7
M0_MA8	F27	Q0A0_8	M0_MA8	L17	Q0A0_8
M0_MA9	A28	Q0A0_9	M0_MA9	K	Q0A0_9
M0_MA10	C28	Q0A0_10	M0_MA10	J14	Q0A0_10
M0_MA11	E27	Q0A0_11	M0_MA11	J11	Q0A0_11
M0_MA12	G26	Q0A0_12	M0_MA12	J13	Q0A0_12
M0_MA13	D26	Q0A0_13	M0_MA13	H11	Q0A0_13
M0_MA14	F25	Q0A0_14	M0_MA14	G11	Q0A0_14
M0_MA15	A25	Q0A0_15	M0_MA15	J16	Q0A0_15
M0_MA16	C25	Q0A0_16	M0_MA16	L15	Q0A0_16
M0_MA17	E25	Q0A0_17	M0_MA17	G14	Q0A0_17
M0_MA18	D24	Q0A0_18	M0_MA18	L16	Q0A0_18
M0_MA19	E23	Q0A0_19	M0_MA19	K	Q0A0_19
M0_MA20	F23	Q0A0_20	M0_MA20	E32	Q0A0_20
M0_MA21	D22	Q0A0_21	M0_MA21	A21	Q0A0_21
M0_MA22	F21	Q0A0_22	M0_MA22	C21	Q0A0_22
M0_MA23	E21	Q0A0_23	M0_MA23	E13	Q0A0_23
M0_MA24	D21	Q0A0_24	M0_MA24	D12	Q0A0_24
M0_MA25	F19	Q0A0_25	M0_MA25	E3	Q0A0_25
M0_MA26	A19	Q0A0_26	M0_MA26	D11	Q0A0_26
M0_MA27	D18	Q0A0_27	M0_MA27	E3	Q0A0_27
M0_MA28	F17	Q0A0_28	M0_MA28	F4	Q0A0_28
M0_MA29	A17	Q0A0_29	M0_MA29	H28	Q0A0_29
M0_MA30	C17	Q0A0_30	M0_MA30	A23	Q0A0_30
M0_MA31	E17	Q0A0_31	M0_MA31	E19	Q0A0_31
M0_MA32	D16	Q0A0_32	M0_MA32	E18	Q0A0_32
M0_MA33	F15	Q0A0_33	M0_MA33	D10	Q0A0_33
M0_MA34	A15	Q0A0_34	M0_MA34	D6	Q0A0_34
M0_MA35	D14	Q0A0_35	M0_MA35	G5	Q0A0_35
M0_MA36	F13	Q0A0_36	M0_MA36	H27	Q0A0_36
M0_MA37	A13	Q0A0_37	M0_MA37	A27	Q0A0_37
M0_MA38	C13	Q0A0_38	M0_MA38	C13	Q0A0_38
M0_MA39	E11	Q0A0_39	M0_MA39	G15	Q0A0_39
M0_MA40	A11	Q0A0_40	M0_MA40	E9	Q0A0_40
M0_MA41	C11	Q0A0_41	M0_MA41	H4	Q0A0_41
M0_MA42	A9	Q0A0_42	M0_MA42	L18	Q0A0_42
M0_MA43	C9	Q0A0_43	M0_MA43	K16	Q0A0_43
M0_MA44	F9	Q0A0_44	M0_MA44	H26	Q0A0_44
M0_MA45	D8	Q0A0_45	M0_MA45	H25	Q0A0_45
M0_MA46	E7	Q0A0_46	M0_MA46	G9	Q0A0_46
M0_MA47	A7	Q0A0_47	M0_MA47	G8	Q0A0_47
M0_MA48	C7	Q0A0_48	M0_MA48	G22	Q0A0_48
M0_MA49	F7	Q0A0_49	M0_MA49	G17	Q0A0_49
M0_MA50	A5	Q0A0_50	M0_MA50	G19	Q0A0_50
M0_MA51	E5	Q0A0_51	M0_MA51	G16	Q0A0_51
M0_MA52	C3	Q0A0_52	M0_MA52	H22	Q0A0_52
M0_MA53	E1	Q0A0_53	M0_MA53	J22	Q0A0_53
M0_MA54	G1	Q0A0_54	M0_MA54	J22	Q0A0_54
M0_MA55	G6	Q0A0_55	M0_MA55	G13	Q0A0_55
M0_MA56	G1	Q0A0_56	M0_MA56	K13	Q0A0_56
M0_MA57	G3	Q0A0_57	M0_MA57	K20	Q0A0_57
M0_MA58	G1	Q0A0_58	M0_MA58	J17	Q0A0_58
M0_MA59	G1	Q0A0_59	M0_MA59	G25	Q0A0_59
M0_MA60	J6	Q0A0_60	M0_MA60	H10	Q0A0_60
M0_MA61	J1	Q0A0_61	M0_MA61	H10	Q0A0_61
M0_MA62	J6	Q0A0_62	M0_MA62	H10	Q0A0_62
M0_MA63	J6	Q0A0_63	M0_MA63	H10	Q0A0_63
M0_MA64	J6	Q0A0_64	M0_MA64	H10	Q0A0_64
M0_MA65	J6	Q0A0_65	M0_MA65	H10	Q0A0_65
M0_MA66	J6	Q0A0_66	M0_MA66	H10	Q0A0_66
M0_MA67	J6	Q0A0_67	M0_MA67	H10	Q0A0_67
M0_MA68	J6	Q0A0_68	M0_MA68	H10	Q0A0_68
M0_MA69	J6	Q0A0_69	M0_MA69	H10	Q0A0_69
M0_MA70	J6	Q0A0_70	M0_MA70	H10	Q0A0_70
M0_MA71	J6	Q0A0_71	M0_MA71	H10	Q0A0_71
M0_MA72	J6	Q0A0_72	M0_MA72	H10	Q0A0_72
M0_MA73	J6	Q0A0_73	M0_MA73	H10	Q0A0_73
M0_MA74	J6	Q0A0_74	M0_MA74	H10	Q0A0_74
M0_MA75	J6	Q0A0_75	M0_MA75	H10	Q0A0_75
M0_MA76	J6	Q0A0_76	M0_MA76	H10	Q0A0_76
M0_MA77	J6	Q0A0_77	M0_MA77	H10	Q0A0_77
M0_MA78	J6	Q0A0_78	M0_MA78	H10	Q0A0_78
M0_MA79	J6	Q0A0_79	M0_MA79	H10	Q0A0_79
M0_MA80	J6	Q0A0_80	M0_MA80	H10	Q0A0_80
M0_MA81	J6	Q0A0_81	M0_MA81	H10	Q0A0_81
M0_MA82	J6	Q0A0_82	M0_MA82	H10	Q0A0_82
M0_MA83	J6	Q0A0_83	M0_MA83	H10	Q0A0_83
M0_MA84	J6	Q0A0_84	M0_MA84	H10	Q0A0_84
M0_MA85	J6	Q0A0_85	M0_MA85	H10	Q0A0_85
M0_MA86	J6	Q0A0_86	M0_MA86	H10	Q0A0_86
M0_MA87	J6	Q0A0_87	M0_MA87	H10	Q0A0_87
M0_MA88	J6	Q0A0_88	M0_MA88	H10	Q0A0_88
M0_MA89	J6	Q0A0_89	M0_MA89	H10	Q0A0_89
M0_MA90	J6	Q0A0_90	M0_MA90	H10	Q0A0_90
M0_MA91	J6	Q0A0_91	M0_MA91	H10	Q0A0_91
M0_MA92	J6	Q0A0_92	M0_MA92	H10	Q0A0_92
M0_MA93	J6	Q0A0_93	M0_MA93	H10	Q0A0_93
M0_MA94	J6	Q0A0_94	M0_MA94	H10	Q0A0_94
M0_MA95	J6	Q0A0_95	M0_MA95	H10	Q0A0_95
M0_MA96	J6	Q0A0_96	M0_MA96	H10	Q0A0_96
M0_MA97	J6	Q0A0_97	M0_MA97	H10	Q0A0_97
M0_MA98	J6	Q0A0_98	M0_MA98	H10	Q0A0_98
M0_MA99	J6	Q0A0_99	M0_MA99	H10	Q0A0_99
M0_MA100	J6	Q0A0_100	M0_MA100	H10	Q0A0_100



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				LA-F122P			0.03/06		
				Date:	Thursday, November 09, 2017	ISheet	46	of	61

Power-Up/Down Sequence

1. All the ASIC supplies must reach their respective nominal voltages within 20 ms of the start of the ramp-up sequence, though a shorter ramp-up duration is preferred. The maximum slew rate on all rails is 50 mV/ μ s.
2. It is recommended that the 3.3-V rail ramp up first.
3. It is recommended that the 0.95-V rail reach at least 90% of its nominal value no later than 2 ms from the start of VDDC ramping up.
4. The power rails that are shared with other components on the system should be gated for the dGPU so that when the dGPU is powered down (for example AMD PowerXpress? idle state), all the power rails are removed from the dGPU. The gate circuits must meet the slew rate requirement (such as ? 50 mV/ μ s).
5. VDDC and VDD_CT should not ramp up simultaneously. For example, VDDC should reach 90% before VDD_CT starts to ramp up (or vice versa).
6. For power down, reversing the ramp-up sequence is recommended.

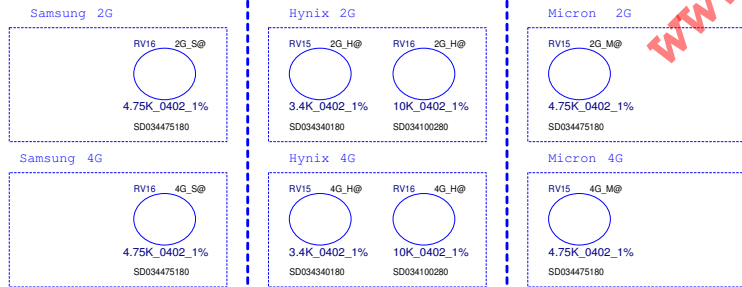
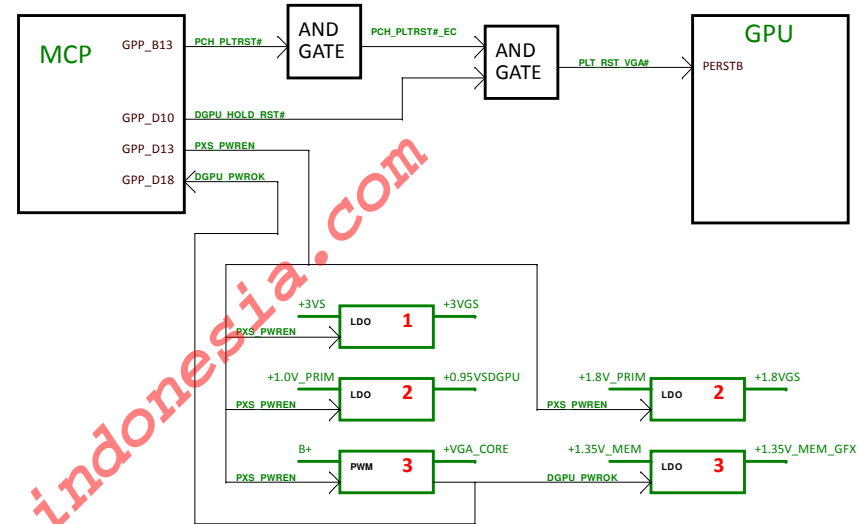
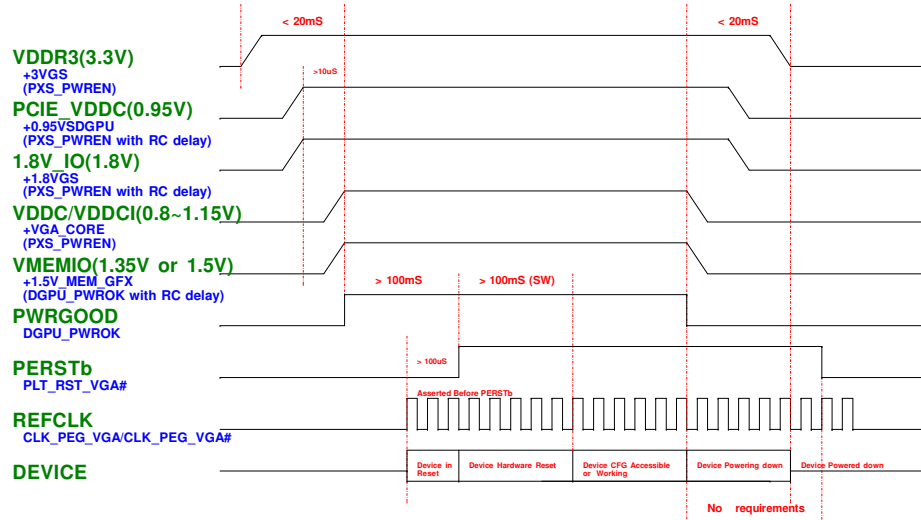


Table 3-21 Resistor Divider Lookup T

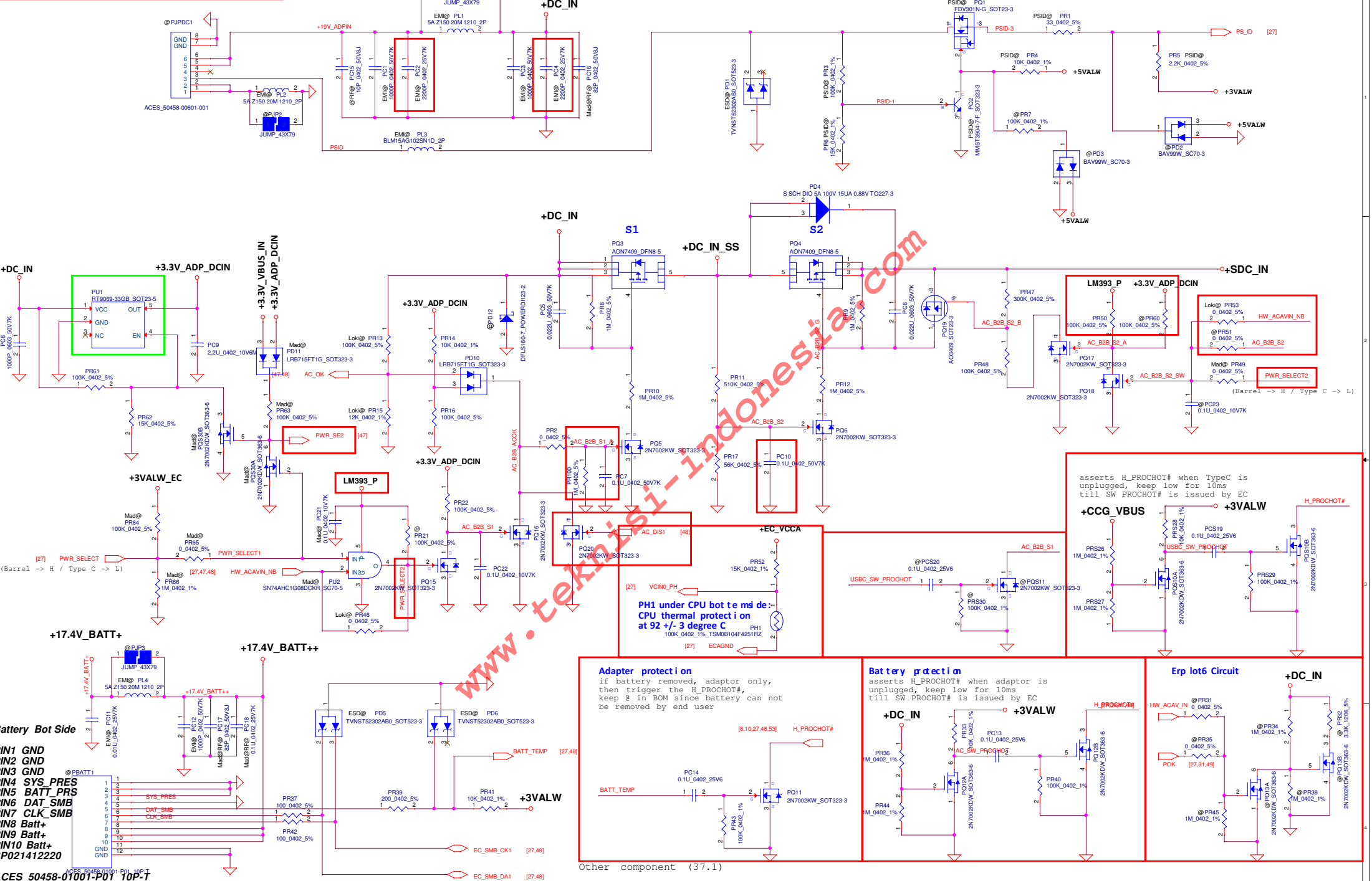
R_pu (Ω)	R_pd (Ω)	Bits [3:1]
NC	4750	000
8450	2000	001
4530	2000	010
6980	4990	011
4530	4990	100
3240	5620	101
3400	10000	110
4750	NC	111

Note: 0402 1% resistors are required.

For AMD R17M-M2-50 VRAM Only

Memory ID	R3 P/N	Vendor	Configuration	Size
000	SA00009TT1L	SAMSUNG	S IC D5 128M32 K4G41325FE-HC28 FBGA A31!	2GB
110	SA00008HQ1L	Hynix	S IC D5 128M32/3G H5GC4H24AJR-R0C A31!	2GB
111	SA00009E31L	Micron	S IC D5 128M32 EDW4032BABG-70-F-R A31!	2GB

Main Func = DCIN/BATT CONN



Battery Bot Side

PIN1 GND
PIN2 GND
PIN3 GND
PIN4 SYS_PRES
PIN5 BATT_PRS
PIN6 DAT_SMB
PIN7 CLK_SMB
PIN8 Batt+
PIN9 Batt+
PIN10 Batt+
SP021412220

ACES_50458-01001-P01_10P-T

Adapter protection

if battery removed, adaptor only, then trigger the H_PROCHOT#, keep 0 in BOM since battery can not be removed by end user

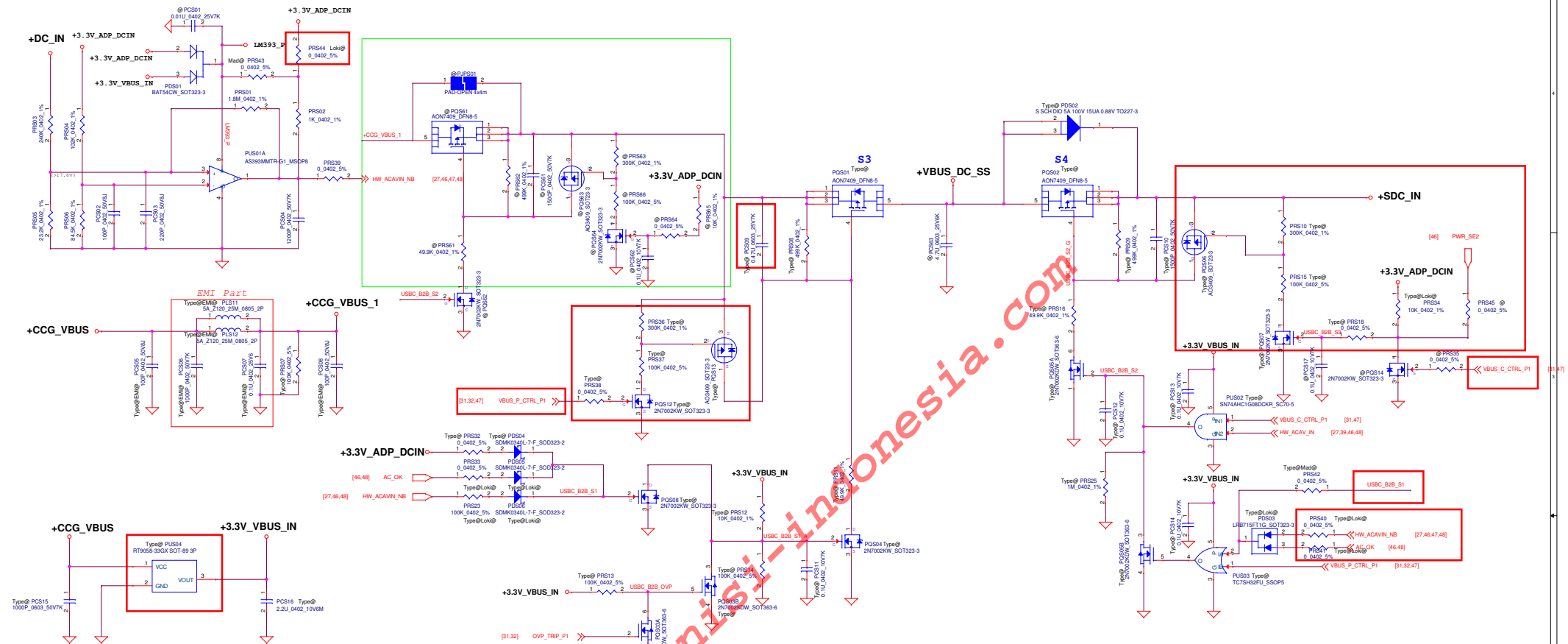
Battery protection

asserts H_PROCHOT# when adaptor is unplugged, keep low for 10ms till SW_PROCHOT# is issued by EC

Erp lot6 Circuit

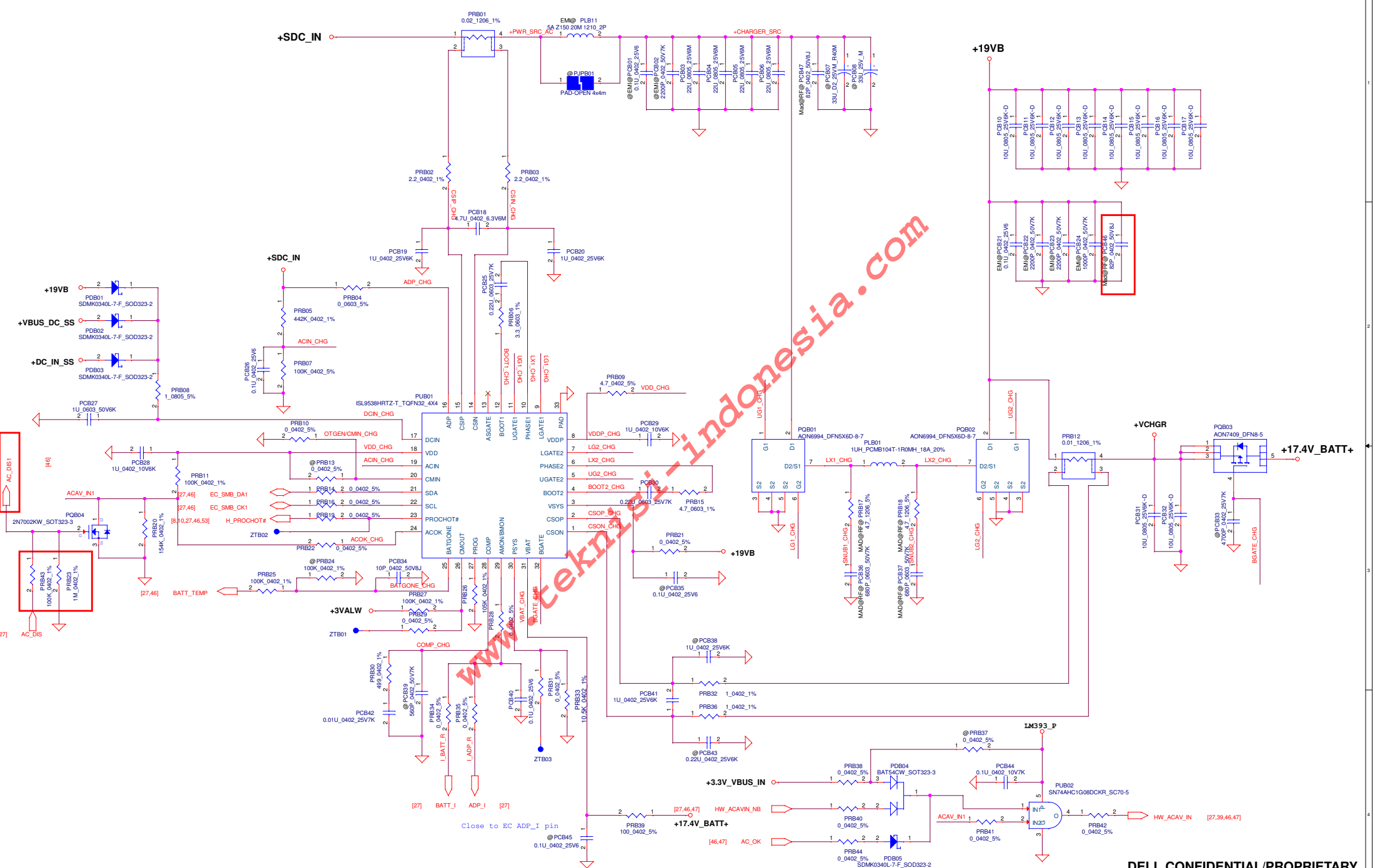
Main Func = Type-C PD Selector

DCIN_AC_Detector

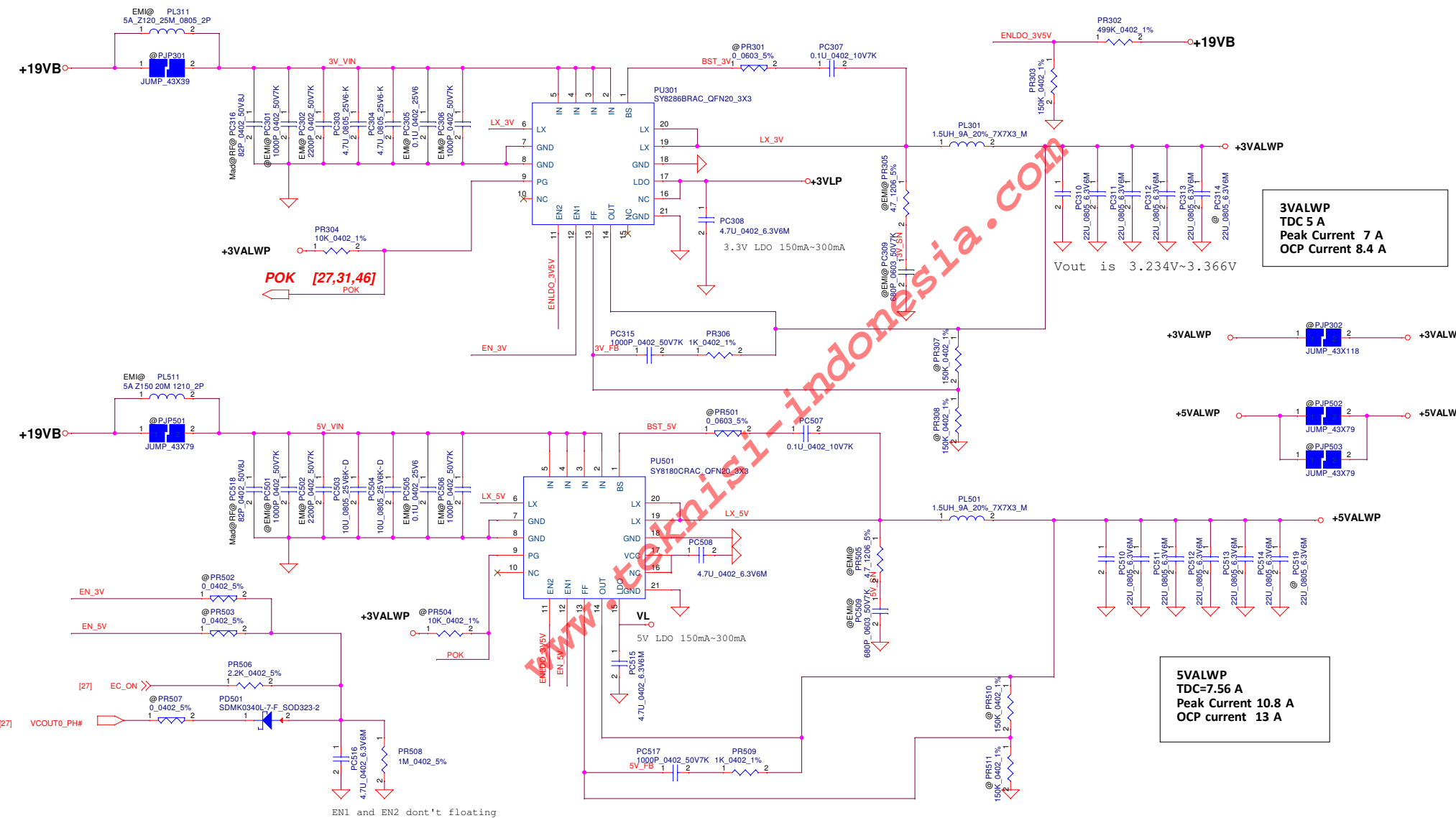


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			Rev 000	
			Date: Thursday, November 02, 2017	Sheet 47 of 59

Main Func = CHARGER

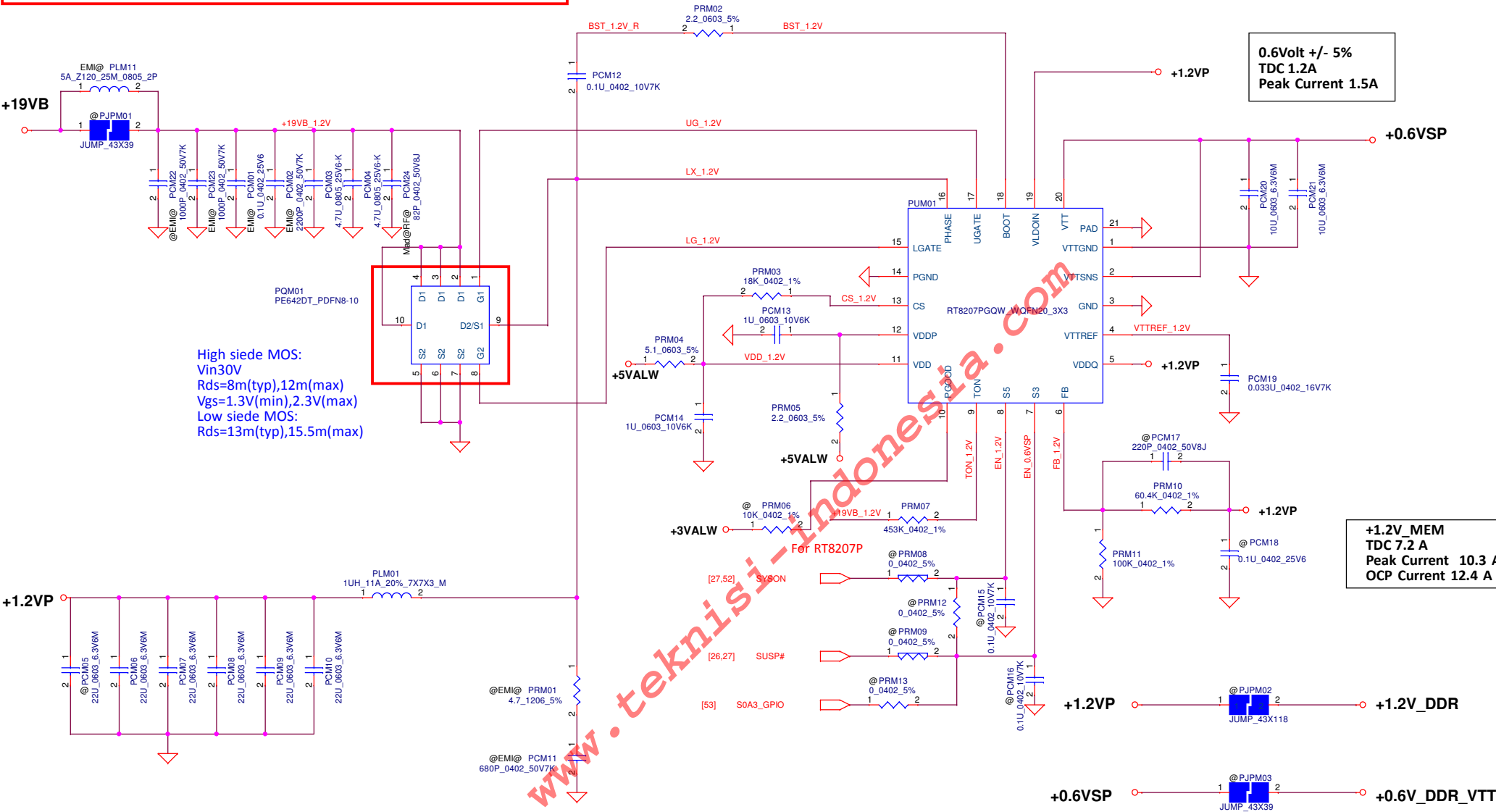


Main Func = 3.3VALWP/5VALWP



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Main Func = +1.2V_DDR/+0.6V_DDR_VTT



High side MOS:
Vin30V
Rds=8m(typ),12m(max)
Vgs=1.3V(min),2.3V(max)
Low side MOS:
Rds=13m(typ),15.5m(max)

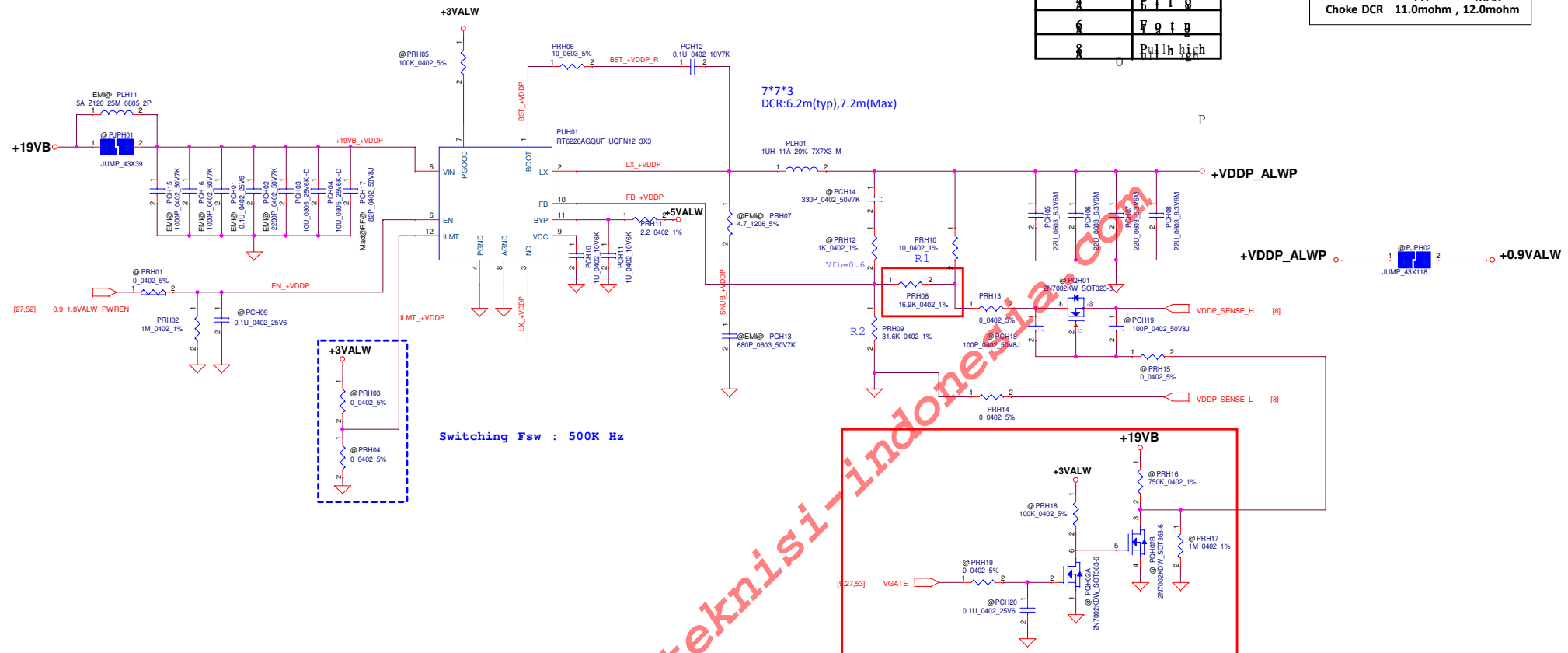
Mode	S3	S5	+1.2V_MEN	+V_DDR_REF	+0.6V_P
S5	L	L	off	off	off
S3	L	H	on	on	off
S0	H	H	on	on	on

Main Func = +VDDP_ALWP

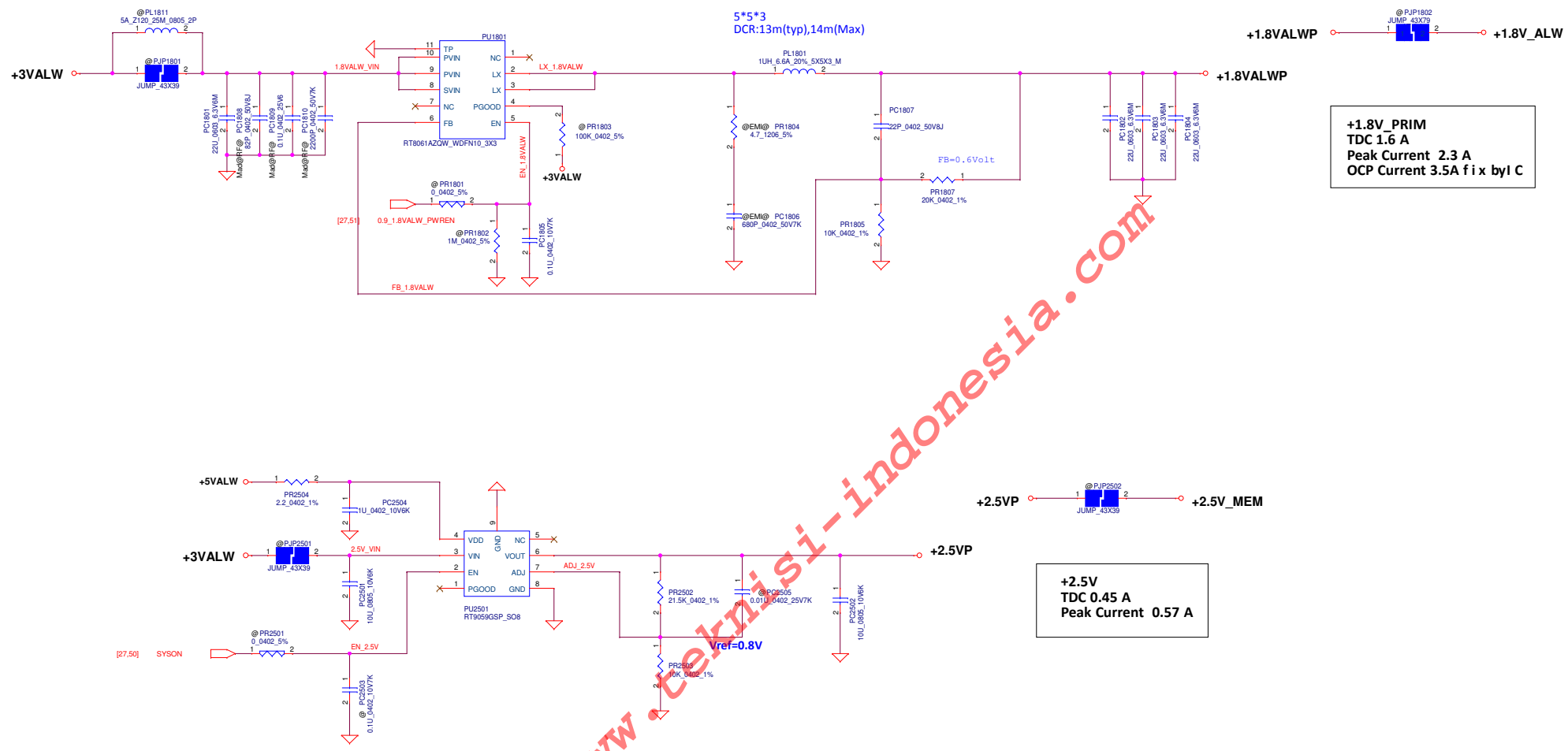
The current limit is set to 4A, 6A or 8A when this pin is pull low, floating or pull high

OCPS setting	IM pin 3
4	Pin 10
6	Foot 0
8	Pull high

+VDDP_ALWP
TDC 4 A
Peak Current 5 A
OCP Current 6 A Fix by IC
Choke DCR 11.0mohm , 12.0mohm



Main Func = +1.8VALWP / +2.5VP

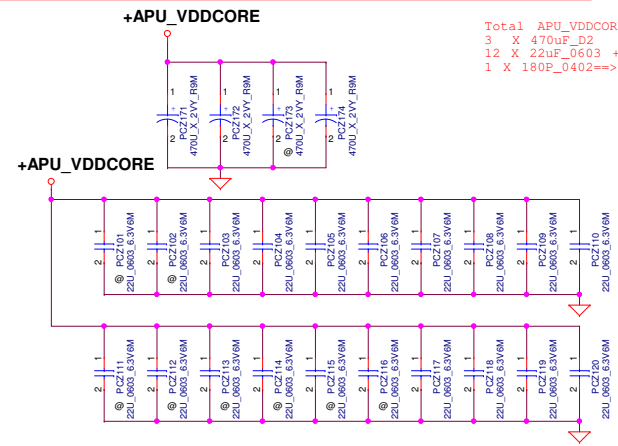


+1.8V PRIM
TDC 1.6 A
Peak Current 2.3 A
OCP Current 3.5A f i x byl C

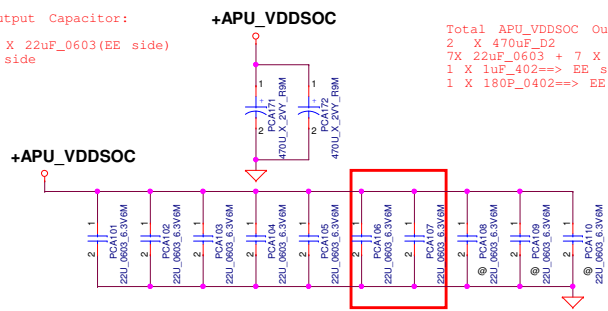
+2.5V
TDC 0.45 A
Peak Current 0.57 A

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2015/03/23		2014/12/15		PWR +1.8V PRIM and +2.5V	
Size		Document Number		Rev	
C				X00	
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Main Func = APU/ VGA / APU_SOC MLCC

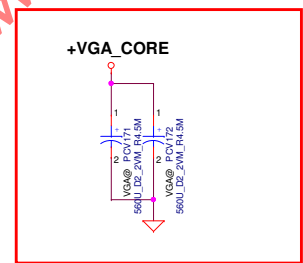


Total APU_VDDCORE Output Capacitor:
3 X 470uF_D2
12 X 22uF_0603 + 16 X 22uF_0603 (EE side)
1 X 180pF_0402==> EE side

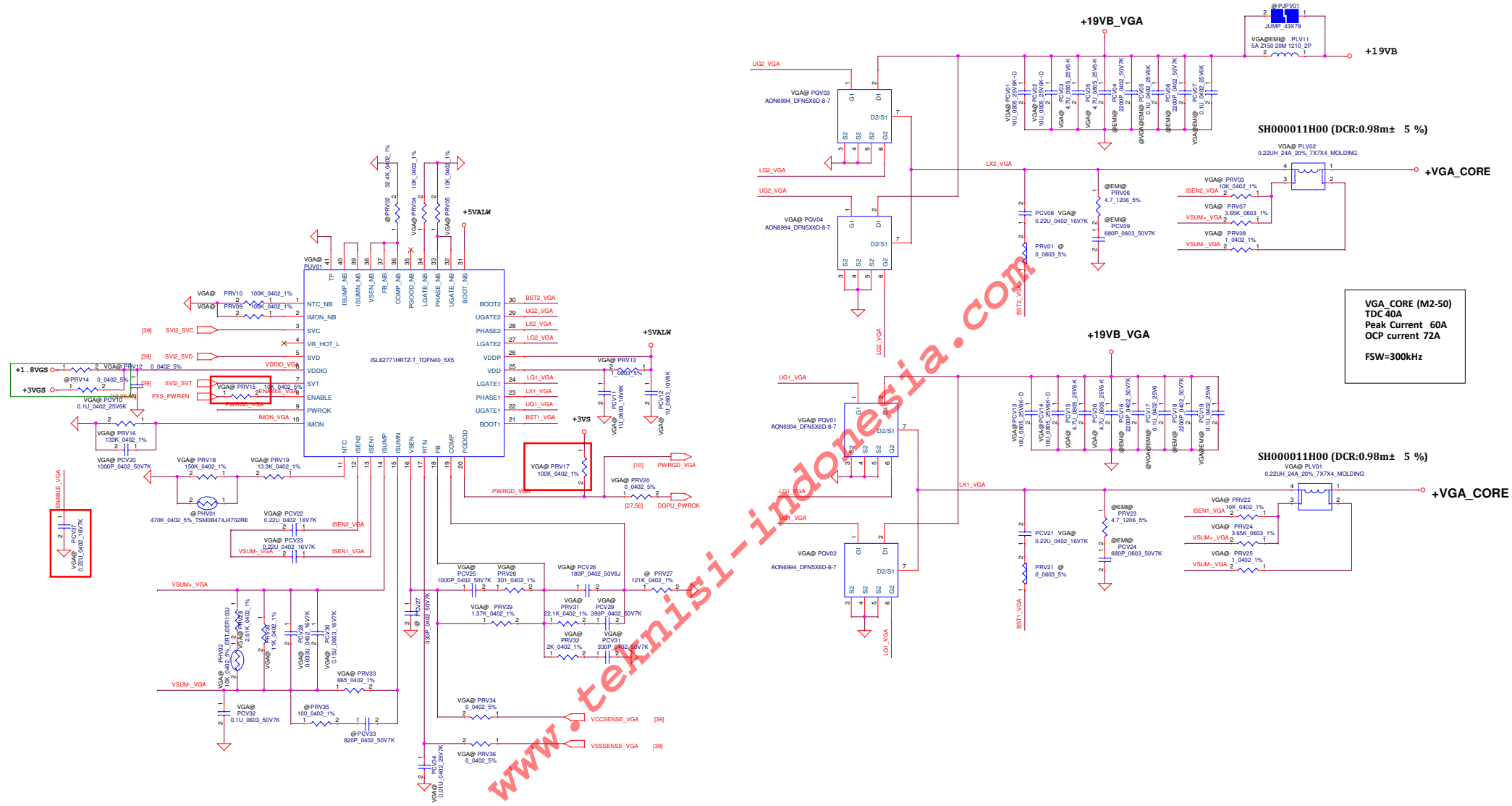


Total APU_VDDSOC Output Capacitor:
2 X 470uF_D2
7X 22uF_0603 + 7 X 22uF_0603 (EE side)
1 X 1uF_402==> EE side
1 X 180pF_0402==> EE side

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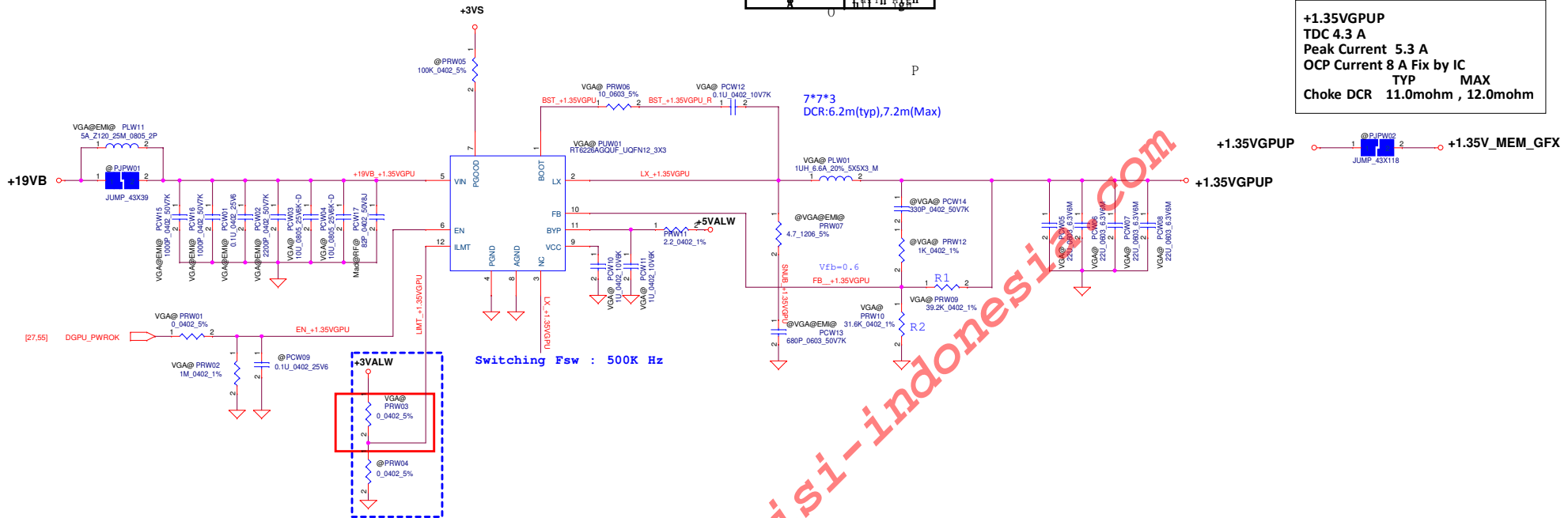
For VGACORE



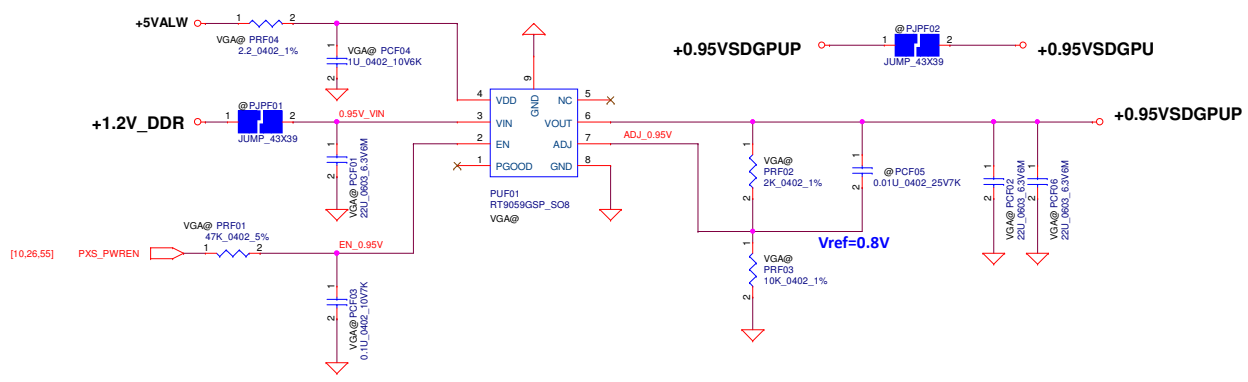
VGA_CORE (M2-50)
TDC 40A
Peak Current 60A
OCP current 72A
FSW=300kHz

Main Func = +1.35VG PUP

CCPs setting	IMPin3
4	Pl 1 0
6	F 9 f p
8	Pullh high



Main Func = +0.95VSDGPUP

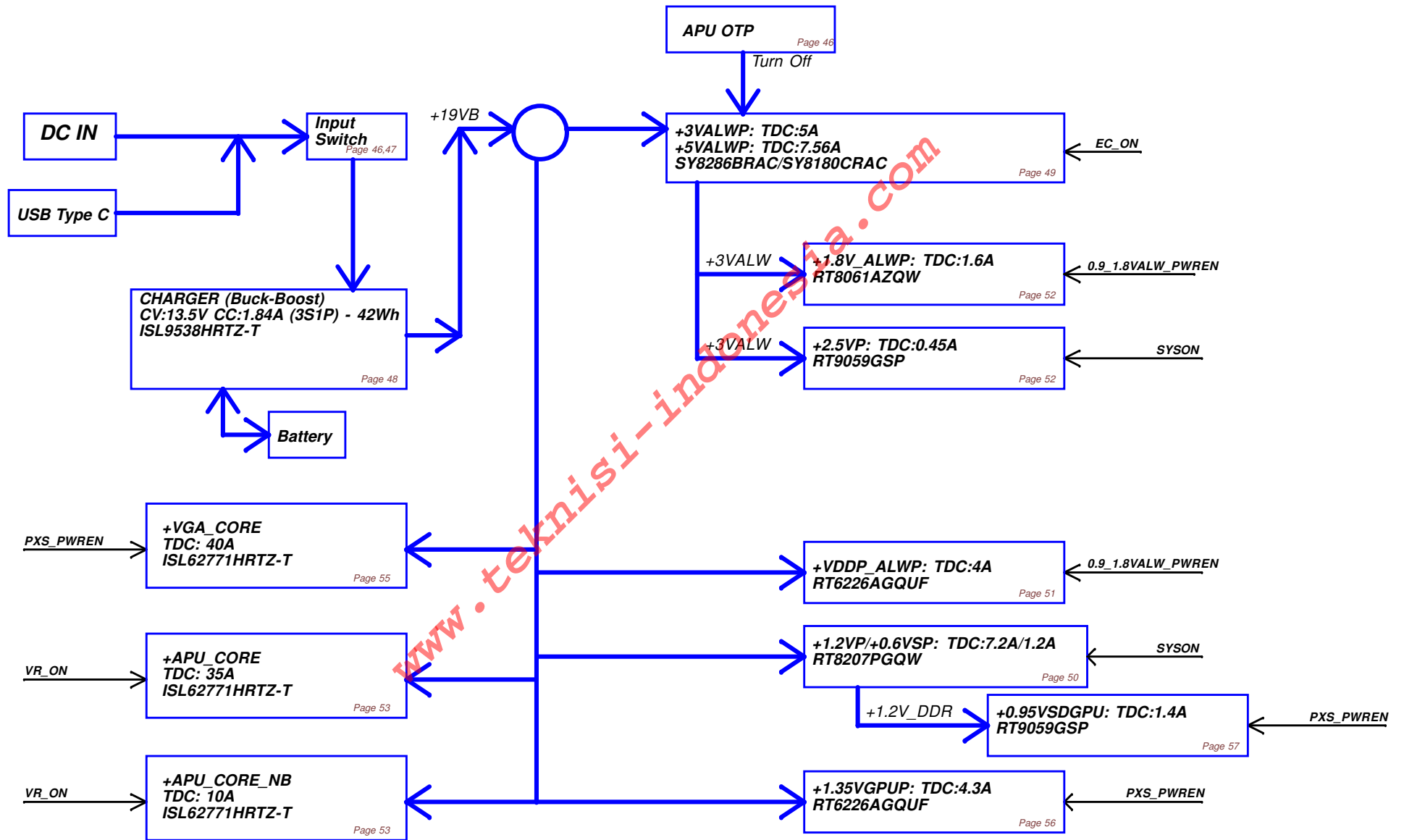


+0.95VSDGPU
TDC 1.4 A
Peak Current 2 A

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Size	Document	Number	Rev	X00
Custom				
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Power block



Version Change List (P. I. R. List)

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	P46	PWR	20170704	COMPAL	EMI test result for change capacity	change PC2,PC4 from 0.1u to 2200p	0.2 (X01)
2	P55	PWR	20170704	COMPAL	Request by EE for adjust DGPU sequence	change PRV15 from 0 to 10K and add PCV37 0.22u	0.2 (X01)
3	P48	PWR	20170704	COMPAL	support FTRD 1.6 and LPS from EC request	change PRV15 from 0 to 10K and add PCV37 0.22u	0.2 (X01)
4	P47	PWR	20170704	COMPAL	add fast close MOS	pop PQS06,PQS07,PQS13,PRS10,PRS15,PRS18,PRS36,PRS37,PRS38,PRS40.PRS41	0.2 (X01)
5	P46	PWR	20170710	COMPAL	for LPS SW solution	add PQ20	0.2 (X01)
6	P51	PWR	20170717	COMPAL	adjust output to 0.9V by EE request	change PRH08 from 10.7K to 15.8K	0.2 (X01)
7	P46	PWR	20170917	COMPAL	follow Intel design	pop PR53 and unpop PR51	0.3 (X02)
8	P46	PWR	20170917	COMPAL	follow Intel design	unpop PC23,PQS11,PRS30,PCS20 add PR100 1M	0.3 (X02)
9	P54	PWR	20170918	COMPAL	for PSI_Dynamic test with AMD validation	pop PCA106,PCA107	0.3 (X02)
10	P48	PWR	20170918	COMPAL	follow Intel design	unpop PCB46	0.3 (X02)
11	P51	PWR	20170918	COMPAL	for VDDP_Static test with AMD validation	change PRH08 from 15.8K to 16.9K	0.3 (X02)
12	P46	PWR	20170920	COMPAL	follow Intel design	change PC7,PC10 from 0.1U_10V to 0.1U_50V	0.3 (X02)
13							
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DVT2 change list

BOM change list

BOM Change								
Item		Date	Page	Part reference	Original CPN	New CPN	Change description	Reason
1		2017/9/4	32	D2	SCA00001G00		unpop	follow ESD require
4		2017/9/4	27	RE9	SD034150280	SD034270280	15K change to 27K	EC board ID
5		2017/9/4	27	RE9	SD034200280	SD034330280	20K change to 33K	EC board ID
12		2017/9/4	11	RC801	SD028100580		add 10M	follow factory require for RTC detect
13		2017/9/4	11	QC27	SB00000EN00		add mos	follow factory require for RTC detect
14		2017/9/4	9	RC6130	SD028100280		add 10K	follow factory require for RTC detect
15		2017/9/8	18	CA50.CA51	SE071100180		change to pop	follow EMI require
16		2017/9/18	33	RT132,RT133	SD028000080		add 0 ohm	follow SCL1.05

GPIO change list

Signal for PCH									
Date	GPIO	Pin Definition		Reason					
		R0.2(X01)	R0.3(X02)						
	AGPIO7	NC	RTC_DET#	factory require					
	AGPIO76	SPI_IRQ#	NC	PSP related GPIO					
	AGPIO30	NC	SPI_IRQ#	PSP related GPIO					
	EGPIO121	BT_ON#	NC	BITS339503 DVT1-Loki-AMD:1810 WLAN/BT device lost after resume from S3/S4/CB/WB.					
	EGPIO120	NC	BT_ON#	BITS339503 DVT1-Loki-AMD:1810 WLAN/BT device lost after resume from S3/S4/CB/WB.					

Design change list

Design Change							
Item	Date	Page	Part reference	change description	Reason		
Based on DVT1							
1	2017/9/4	11	QC27.RC801.RC6130	add RTC coin battery detect circuit	for factory require		
2	2017/9/4	27	RE9	UMA form 15K to 27K, DIS from 20K to 33K	EC board ID		
3	2017/9/4	10,20	RC902	reserve (0 ohm)	BITS339503 DVT1-Loki-AMD:1810 WLAN/BT device lost after resume from S3/S4/CB/WB.		
4	2017/9/12			I2C0 change to I2C3	BITS332966 ULV-Loki-AMD: Lost some items in Touchpad setting.		
5	2017/9/18	33	RT132,RT133	add series resistor for APU_DP3_AUXP/APU_DP3_AUXN	follow SCL 1.05		